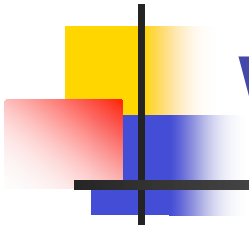
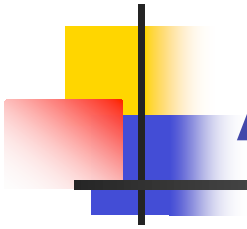
What is ADC

- An electronic integrated circuit which transforms a signal from analog (continuous) to digital (discrete) form.
- Analog signals are directly measurable quantities.
- Digital signals only have two states. For digital computer, we refer to binary states, 0 and 1.



Why ADC is needed

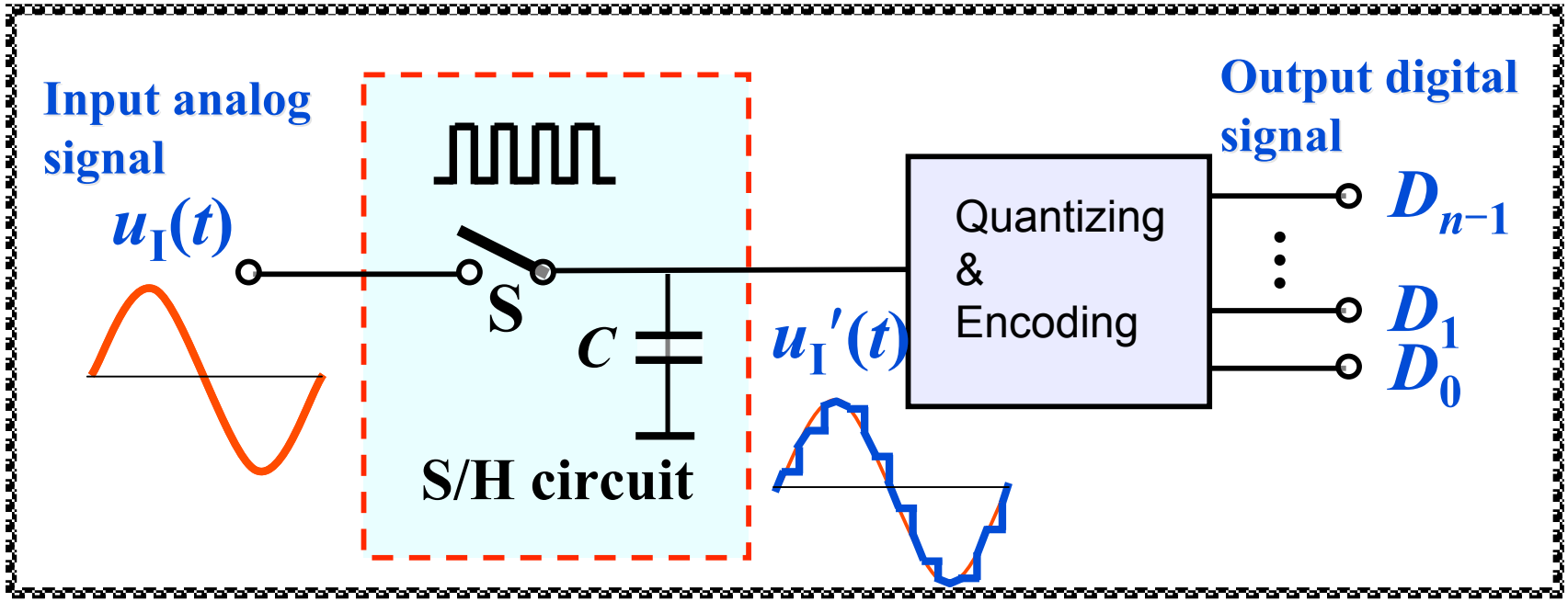
- Microprocessors can only perform complex processing on digitized signals.
- When signals are in digital form they are less susceptible to the deleterious effects of additive noise.
- ADC Provides a link between the analog world of transducers and the digital world of signal processing and data handling.



Application of ADC

- ADC are used virtually everywhere where an analog signal has to be processed, stored, or transported in digital form.
- Some examples of ADC usage are digital volt meters, cell phone, thermocouples, and digital oscilloscope.
- Microcontrollers commonly use 8, 10, 12, or 16 bit ADCs, our micro controller uses an 8 or 10 bit ADC.

ADC process

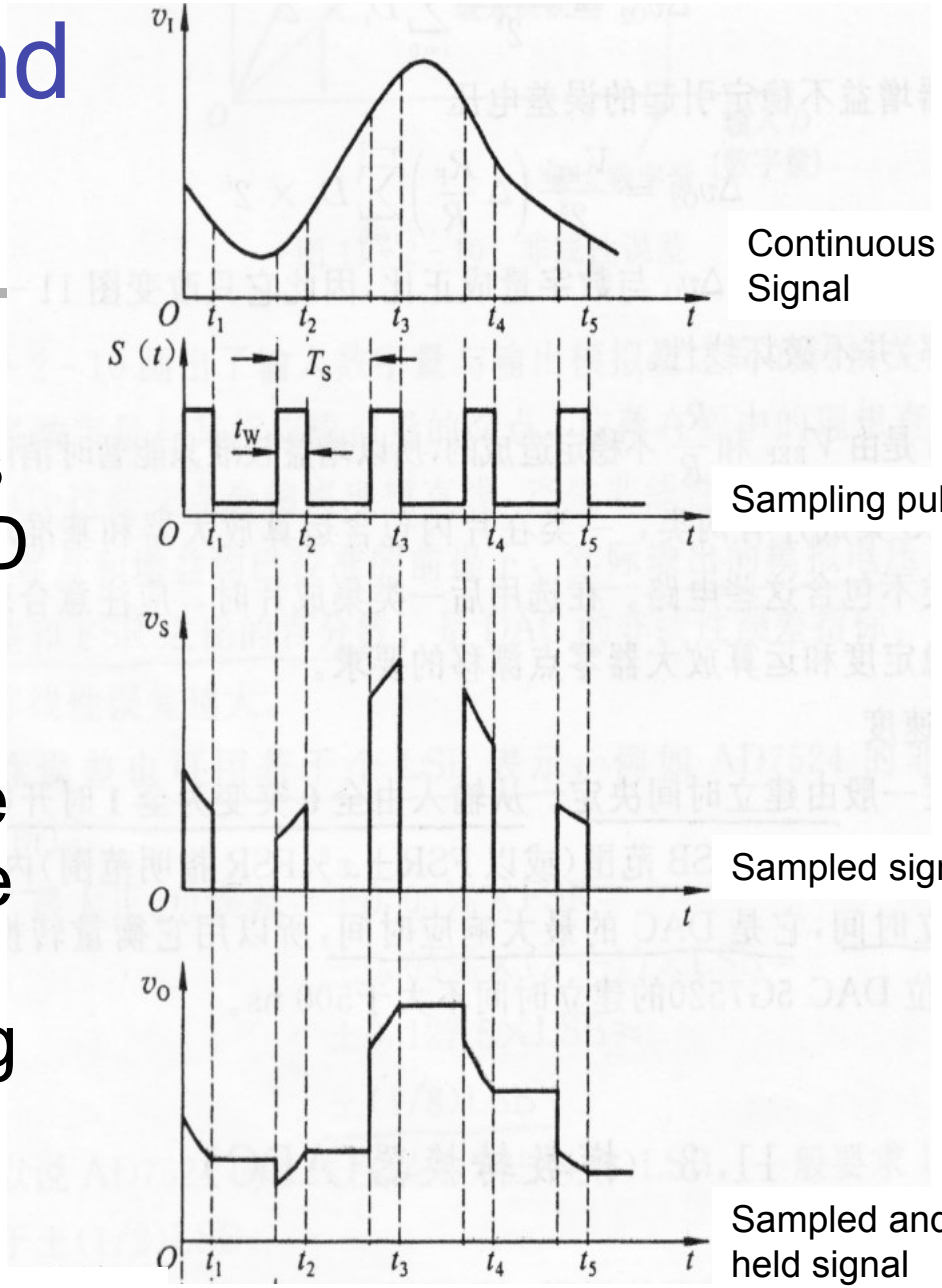


2 steps

- Sampling and Holding (S/H)
- Quantizing and Encoding (Q/E)

Sampling and Holding

- Holding signal benefits the accuracy of the A/D conversion
- Minimum sampling rate should be at least twice the highest data frequency of the analog signal



Quantizing and Encoding

Resolution:

The smallest change in analog signal that will result in a change in the digital output.

$$\Delta V = \frac{V_r}{2^N}$$

V = Reference voltage range

N = Number of bits in digital output.

2^N = Number of states.

ΔV = Resolution

The resolution represents the quantization error inherent in the conversion of the signal to digital form

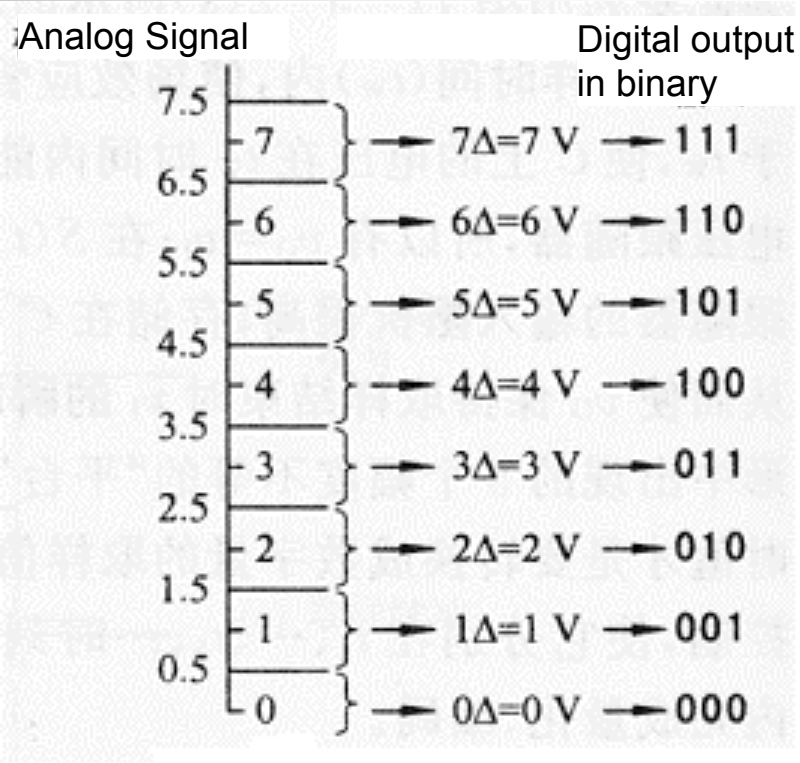
Quantizing and Encoding

- Quantizing:

Partitioning the reference signal range into a number of discrete quanta, then matching the input signal to the correct quantum.

- Encoding:

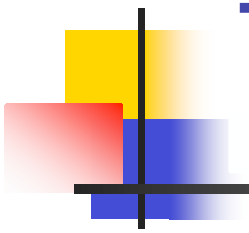
Assigning a unique digital code to each quantum, then allocating the digital code to the input signal.



$$\Delta V = 1\,V$$

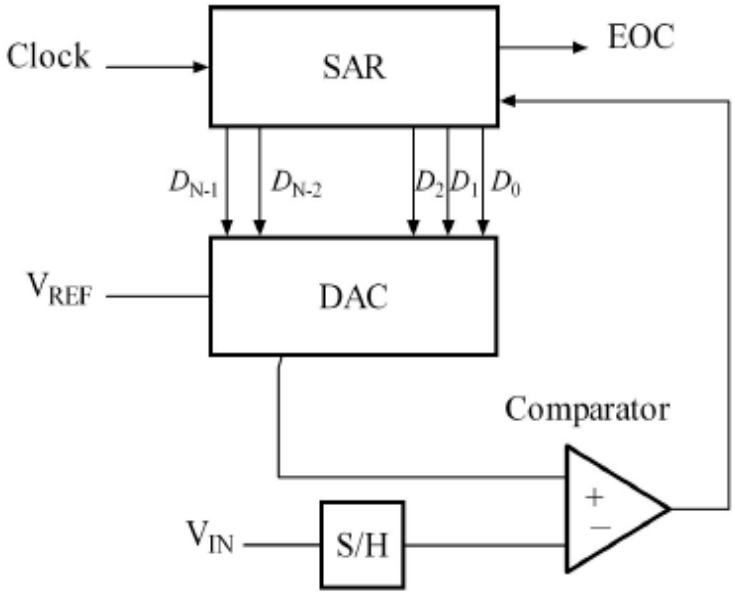
$$\text{Maximum Quantization error} = \pm\frac{1}{2}\Delta V = \pm 0.5\,V$$

Types of A/D Converters



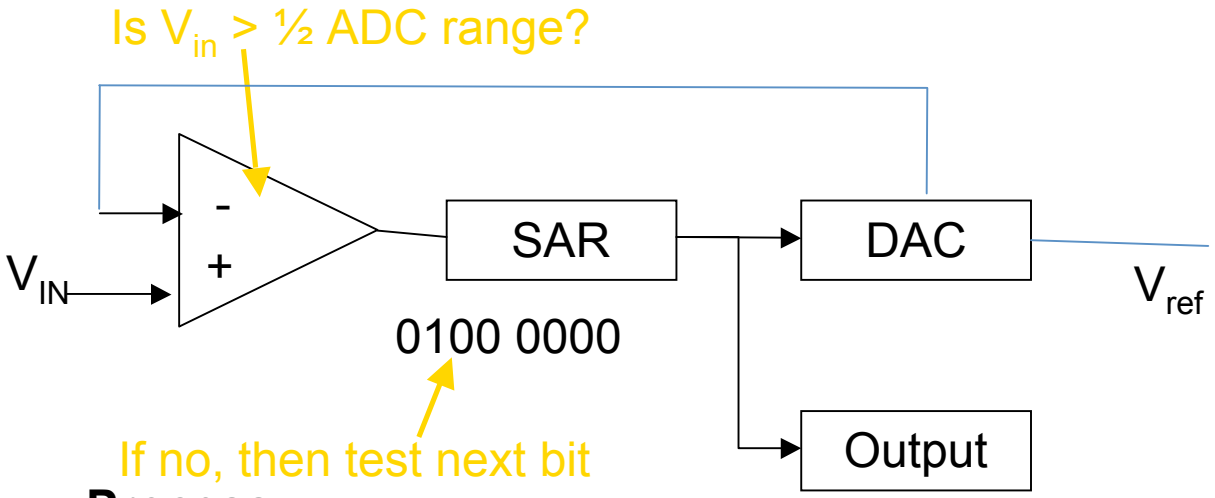
- Dual Slope A/D Converter
- Successive Approximation A/D Converter
- Flash A/D Converter
- Delta-Sigma A/D Converter
- Other
  - Voltage-to-frequency, staircase ramp or single slope, charge balancing or redistribution, switched capacitor, tracking, and synchro or resolver

Successive Approximation ADC Circuit



- Uses a n-bit DAC to compare DAC and original analog results.
- Uses Successive Approximation Register (SAR) supplies an approximate digital code to DAC of Vin.
- Comparison changes digital output to bring it closer to the input value.
- Uses Closed-Loop Feedback Conversion

Successive Approximation ADC

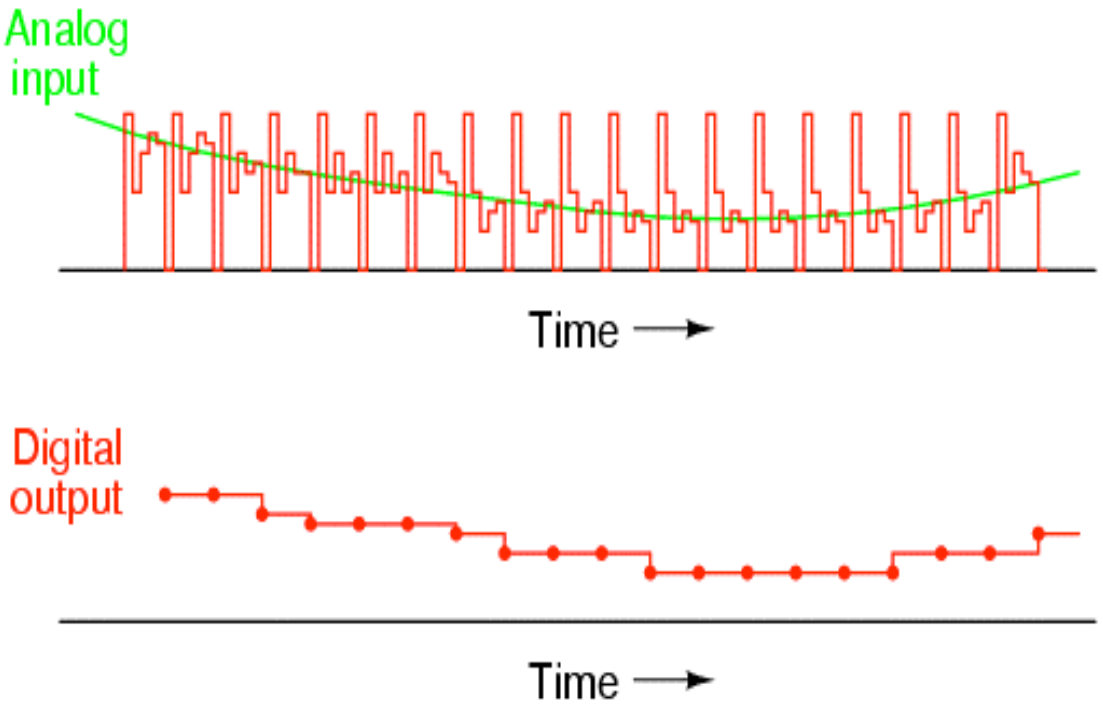


Process

1. MSB initialized as 1
2. Convert digital value to analog using DAC
3. Compares guess to analog input
4. Is V_{in}>V_{DAC}
   - Set bit 1
   - If no, bit is 0 and test next bit

Closed-Loop

Output



Successive Approximation

Advantages

- Capable of high speed and reliable
- Medium accuracy compared to other ADC types
- Good tradeoff between speed and cost
- Capable of outputting the binary number in serial (one bit at a time) format.

Disadvantages

- Higher resolution successive approximation ADC's will be slower
- Speed limited to ~5Msps

Successive Approximation Example

Example

- 10 bit ADC
- Vin= 0.6 volts (from analog device)
- V_{ref}=1 volts
- Find the digital value of Vin

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625

$N=2^n$ (N of possible states)
N=1024
Vmax-Vmin/N = 1 Volt/1024 = 0.0009765625V of Vref (resolution)

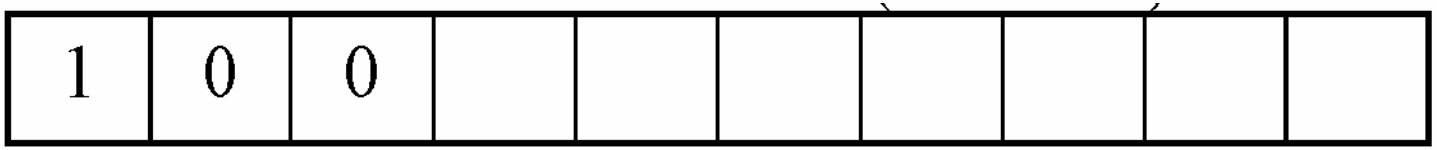
Successive Approximation

- MSB (bit 9)
  - Divided V_{ref} by 2
  - Compare $V_{ref}/2$ with V_{in}
  - If V_{in} is greater than $V_{ref}/2$, turn MSB on (1)
  - If V_{in} is less than $V_{ref}/2$, turn MSB off (0)
  - V_{in} =0.6V and V=0.5
  - Since V_{in}>V, MSB = 1 (on)

Bit	Voltage
9	.5
8	.25
7	.125
6	.0625
5	.03125
4	.015625
3	.0078125
2	.00390625
1	.001952125
0	.0009765625

Successive Approximation

- Next Calculate MSB-1 (bit 8)
  - Compare V_{in}=0.6 V to V=V_{ref}/2 + V_{ref}/4= 0.5+0.25 =0.75V
  - Since 0.6<0.75, MSB is turned off
- Calculate MSB-2 (bit 7)
  - Go back to the last voltage that caused it to be turned on (Bit 9) and add it to V_{ref}/8, and compare with V_{in}
  - Compare V_{in} with (0.5+V_{ref}/8)=0.625
  - Since 0.6<0.625, MSB is turned off



Successive Approximation

- Calculate the state of MSB-3 (bit 6)
  - Go to the last bit that caused it to be turned on (In this case MSB-1) and add it to $V_{ref}/16$, and compare it to V_{in}
  - Compare V_{in} to V= 0.5 + $V_{ref}/16$= 0.5625
  - Since 0.6>0.5625, MSB-3=1 (turned on)

MSB	MSB-1	MSB-2	MSB-3	…					
1	0	0	1						

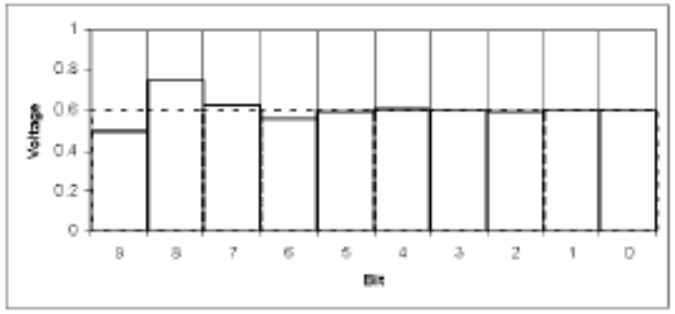
Successive Approximation ADC

- This process continues for all the remaining bits.

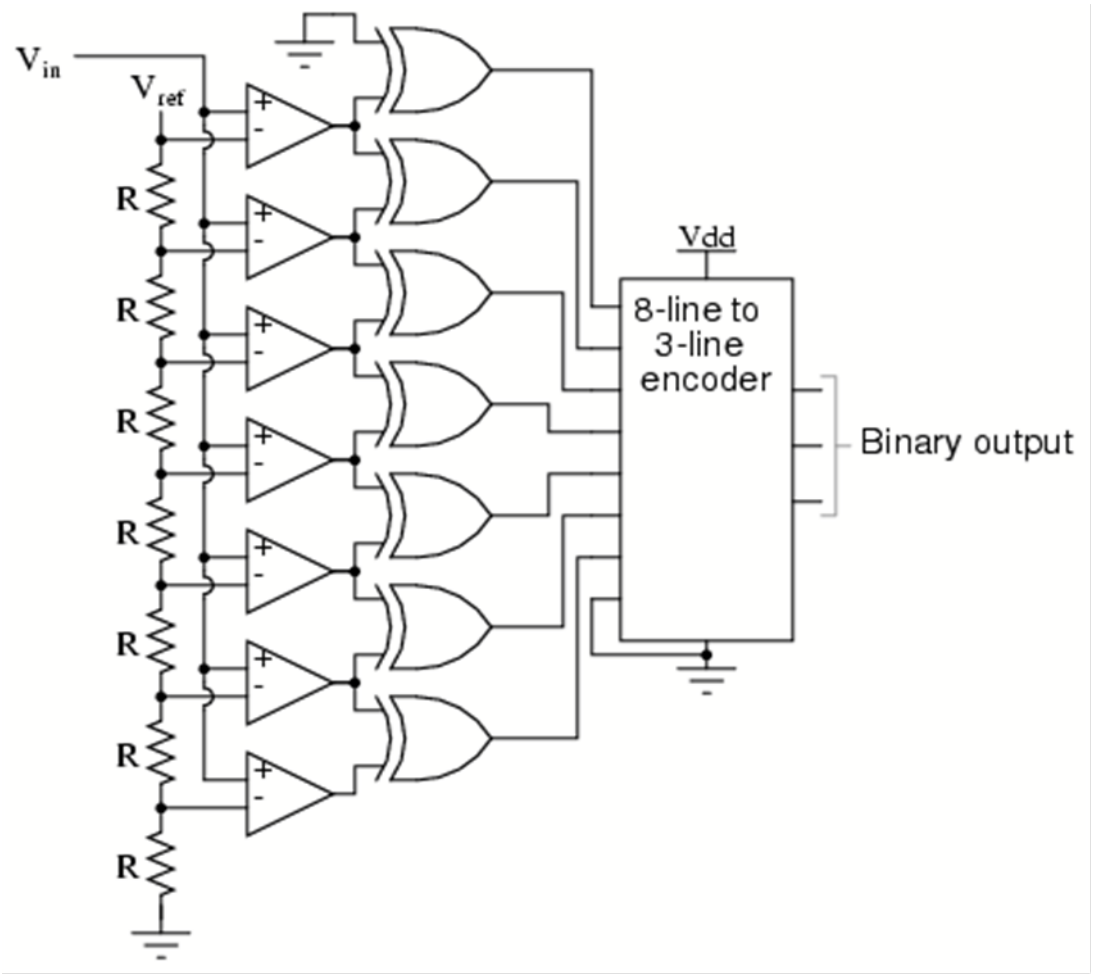
•Digital Results:

MSB	MSB-1	MSB-2	MSB-3	…					LSB
1	0	0	1	1	0	0	1	1	0

•Results: $\frac{1}{2}+\frac{1}{16}+\frac{1}{32}+\frac{1}{256}+\frac{1}{512}=.599609375\ \text{V}$

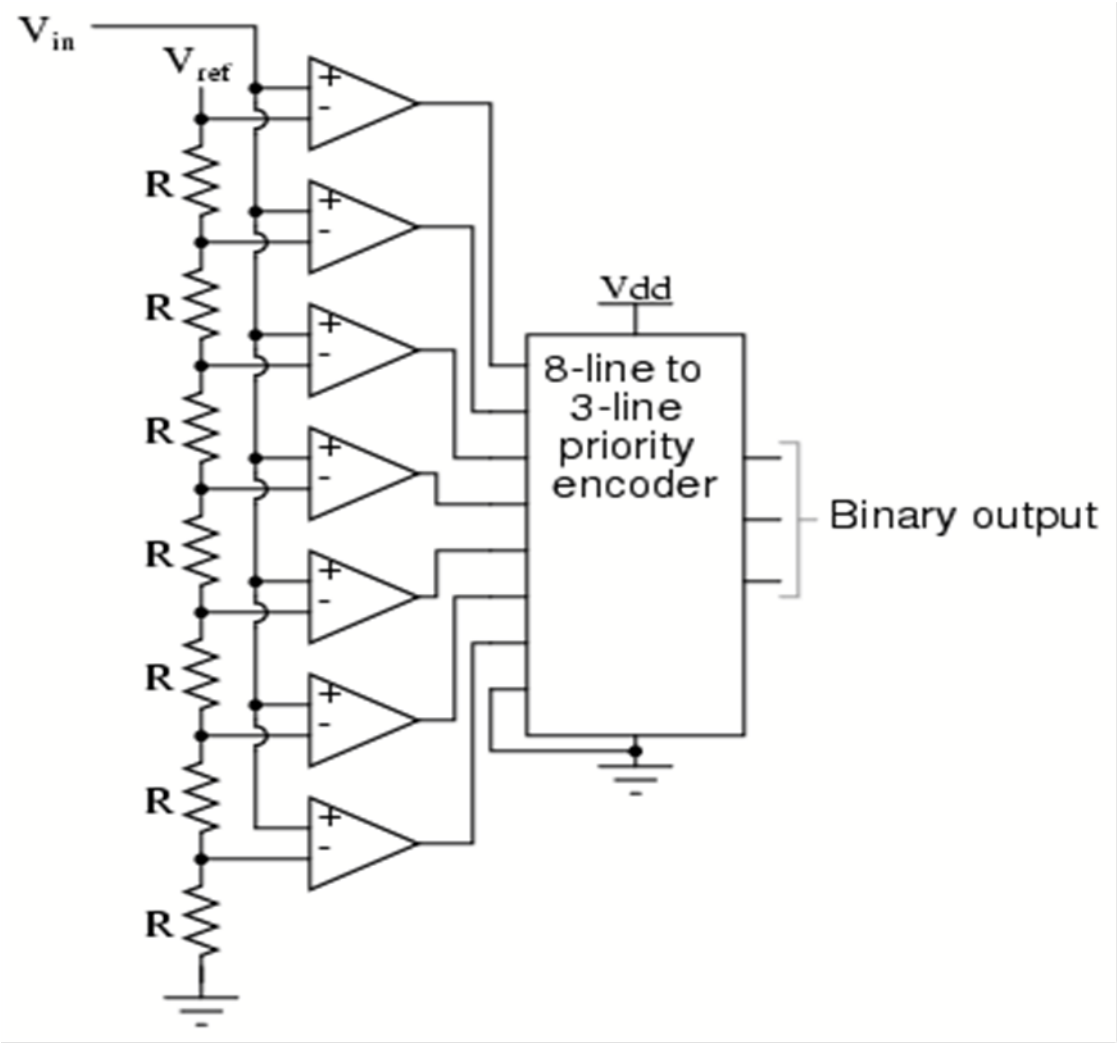


Flash ADC



Flash ADC also called the parallel A/D converter, this circuit is the simplest to understand. It is formed of a series of comparators, each one comparing the input signal to a unique reference voltage.

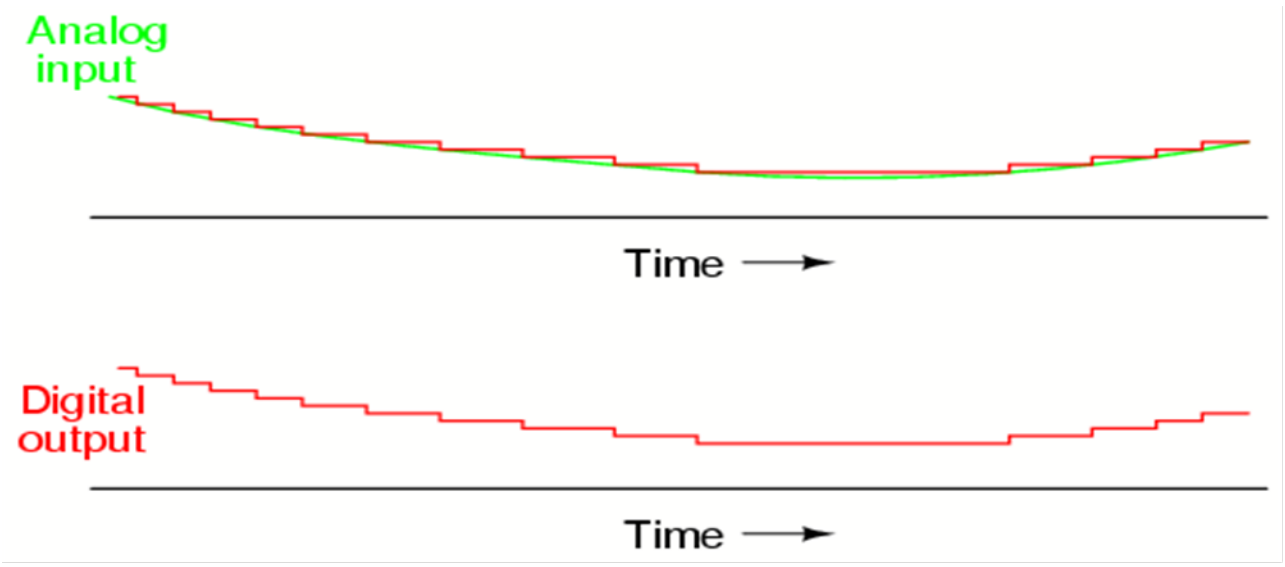
The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output. The following illustration shows a 3-bit flash ADC circuit:



Vref is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit, not shown in the schematic.

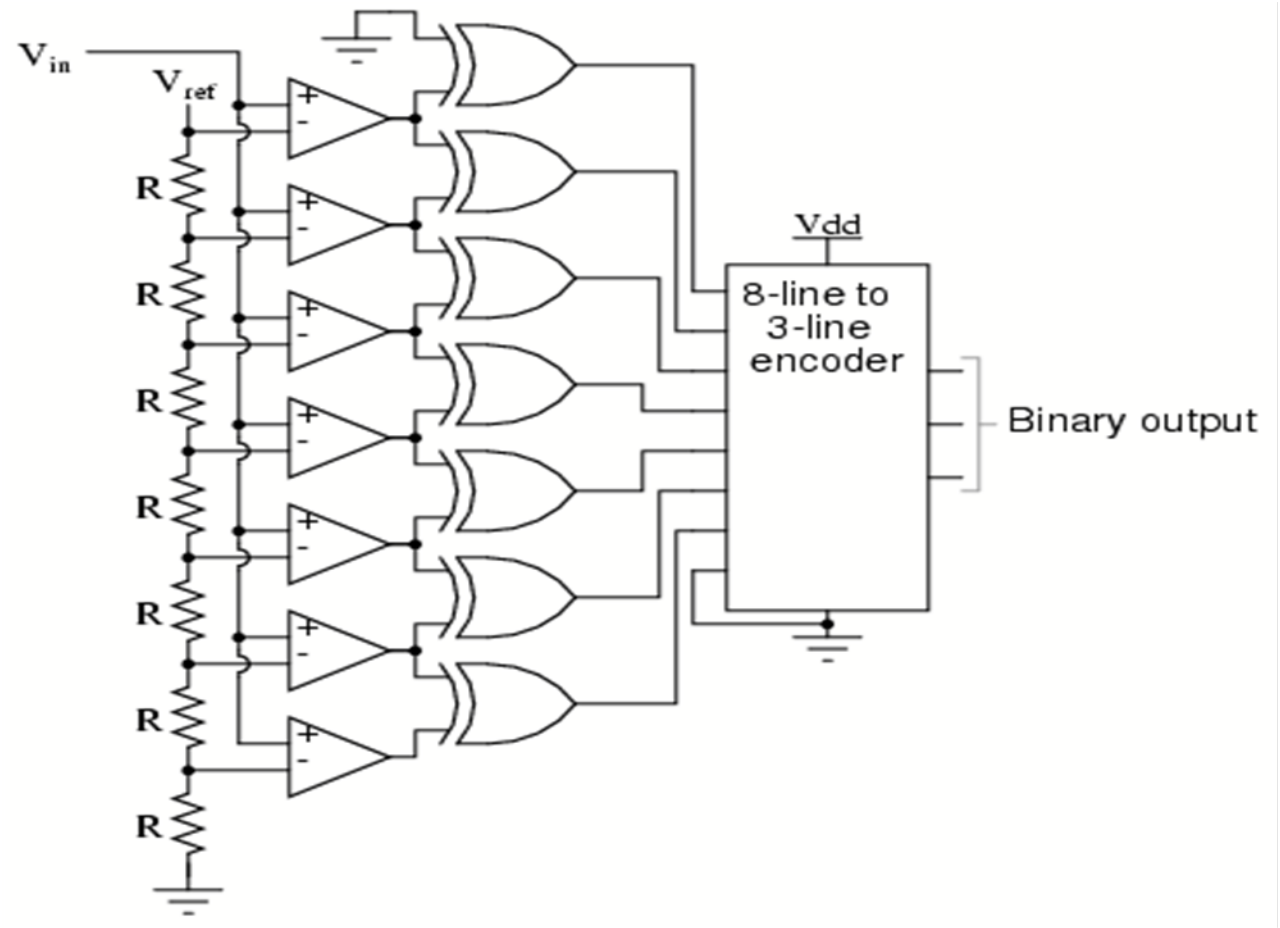
As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

When operated, the flash ADC produces an output that looks something like this:

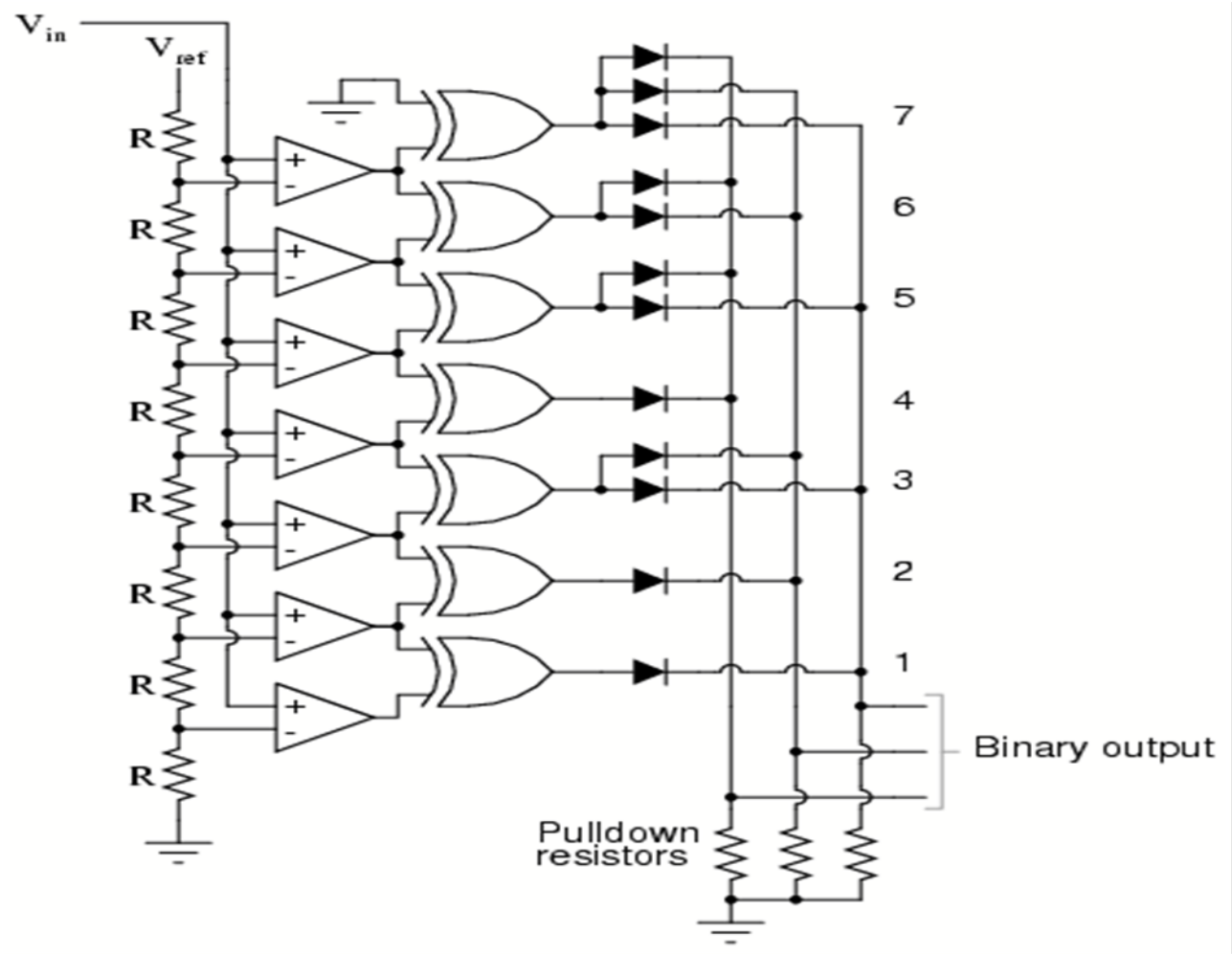


For this particular application, a regular priority encoder with all its inherent complexity isn\'t necessary.

Due to the nature of the sequential comparator output states (each comparator saturating “high” in sequence from lowest to highest), the same “highest-order-input selection” effect may be realized through a set of Exclusive-OR gates, allowing the use of a simpler, non-priority encoder:



And, of course, the encoder circuit itself can be made from a matrix of diodes, demonstrating just how simply this converter design may be constructed:



Not only is the flash converter the simplest in terms of operational theory, but it is the most efficient of the ADC technologies in terms of speed, being limited only in comparator and gate propagation delays. Unfortunately, it is the most component-intensive for any given number of output bits.

This three-bit flash ADC requires seven comparators. A four-bit version would require 15 comparators. With each additional output bit, the number of required comparators doubles.

Considering that eight bits is generally considered the minimum necessary for any practical ADC (255 comparators needed!), the flash methodology quickly shows its weakness.

An additional advantage of the flash converter, often overlooked, is the ability for it to produce a non-linear output. With equal-value resistors in the reference voltage divider network, each successive binary count represents the same amount of analog signal increase, providing a proportional response.

For special applications, however, the resistor values in the divider network may be made non-equal. This gives the ADC a custom, nonlinear response to the analog input signal. No other ADC design is able to grant this signal-conditioning behavior with just a few component value changes.