4.2.4 Interrupt Signals

Interrupt signals are input signals to 8086 MP that cause to stop the execution of its current program and go execute a specified procedure. At the end of the procedure it can return to executing the interrupted program. The interrupt signals of the 8086 microprocessor are:

- **INTR (Interrupt Request)**

  is an active high signal shows there is a service request by and external device. This type of interrupt is maskable and can be made to be ignored by the MP through software control by setting / resetting the **IF** flag bit using (**STI/CLI)** instructions

- **$\overline{\text{INTA}}$(Interrupt Acknowledge)**

  This signal is an output from the MP to device requesting the interrupt. It is a response to the **INTR** signal.

- **NMI (None MaskableInterrupt)**

  It is an active high interrupt signal that cannot be ignored, or masked, by the MP through software control.

- **$\overline{\text{TEST}}$ (Test)**

  Input is examined by the "**Wait**" instruction. If the **TEST** input is **LOW** execution continues, otherwise the processor waits in an "**Idle**" state and does not execute any instruction.

- **RESET (Reset)**

  It causes the processor to immediately terminate its present (reset itself). The signal must be active **HIGH** for at least four clock cycles, switching **RESET** to logic 0 initializes the internal registers of the 8086 and initiate a reset service routine.

4.2.5 DMA Signals

Direct memory access (**DMA**) is a system that can control of the memory system without using CPU. **DMA** signals allow an external device to take control of the system bus and transfer its data to memory without the intervention of the microprocessor. The **DMA** technique is done by the following two signals:

- **HOLD**

  This pin is used by external devices to gain control of the busses. It is an active high signal.

- **HLDA (Hold Acknowledge)**

  In response, the processor completes the job at the hand and outputs **HLDA** interrupt signal via pin 30, which indicates to the external device that it can take control the system bus

4.2.6 Power Signals

There are two power signals in 8086 microprocessor, these are:

- **GND (Ground)** = 0 Volt.
- **Vcc (input voltage)** = +5 Volt.

4.3 Memory Interfacing

A memory stores large numbers of binary words. Since the early 1970s, ICs or semiconductor memory have been the most widely used type of primary memory found in microcomputer. The most common types of memory are: **ROM, EEPROM, SRAM** and **DRAM**.

4.3.1 Memory Pin Connections

1. **Address Connection:** each memory chip have address pin (from A_0 to A_{n-1}) depend on the memory capacity where memory capacity = 2^n.

   For example, a memory device with 10 address pins has its address pin label A_0 to A_9 and its memory address capacity is 2^{10}=1024 byte.

2. **Data Connection pins:** the data connection pins are the points of which data are entered reading. Data pin on memory chips are labeled D_0 through D_7

for an 8-bits wide memory device is often called byte wide memory. Although most chips are eight wide some chips are 16-bits, 4-bits or just 1-bit wide.

Most time the memory referred as its address capacity X data pins connection for example (256K X 8) where the memory address capacity is 256k and the data connection is 8-bit wide (1 byte wide).

3. **Selection Connection:** Each memory chip has an input (sometimes more than one input) that selects or enables the memory device that used to select the chip that will be active or enabled from another chips. This type of input often called chip select ($\overline{CS}$), chip enable ($\overline{CE}$) or simple select ($\overline{S}$) input.

   If the $\overline{CS}$, $\overline{CE}$, or S is active (logic 0) the memory is enabled so it can be read or write operation performs while if it is not active (logic 1) then memory chip is disabled so it cannot perform a read or write operation.

4. **Control Connection:** all memory devices have the same for of control input or inputs.

   In ROM there is one control connection that is $\overline{OE}$ which allows data connection pins of ROM. If $\overline{OE}$ is active (logic 0) as well as the $\overline{CS}$, the output is enabled while if $\overline{OE}$ is inactive then the output is disabled at high impedance.

   In RAM chip has either one one or two control inputs. If there is only one control input, it is often called R/$\overline{W}$ this pin selects the memory operation as read or writes if the $\overline{CS}$ is active.

   If the **RAM** has two control inputs, they are usually labeled $\overline{WE}$ (or $\overline{W}$) or $\overline{OE}$.

4.3.2 Address Decoding

In order to attach a memory device to the microprocessor, it is necessary to decode the address sent from the microprocessor. Decoding makes the memory function at unique section or partition of the memory map (specific chip).

4.3.2.1 Simple NAND Gate Decoder

When the NAND gate is used to decode (2K X 8) EPROM for 8088 microprocessor, as known previously memory capacity = 2^n ⟶ $2K=2^n$ that results in n=11. So the address connections (A_0 – A_{10}) are used to refer to each location in memory so they are connected to EPROM directly, while the reminder high 9 bits are connected to input of the NAND gate decoder. The decoder selects the EPROM one from many 2K-byte sections of the entire 1M-byte address range of the 8088 microprocessor as shown in figure (4.3) using simple NAND gate decoder to select EPROM for memory locations (FF800h – FFFFFh).

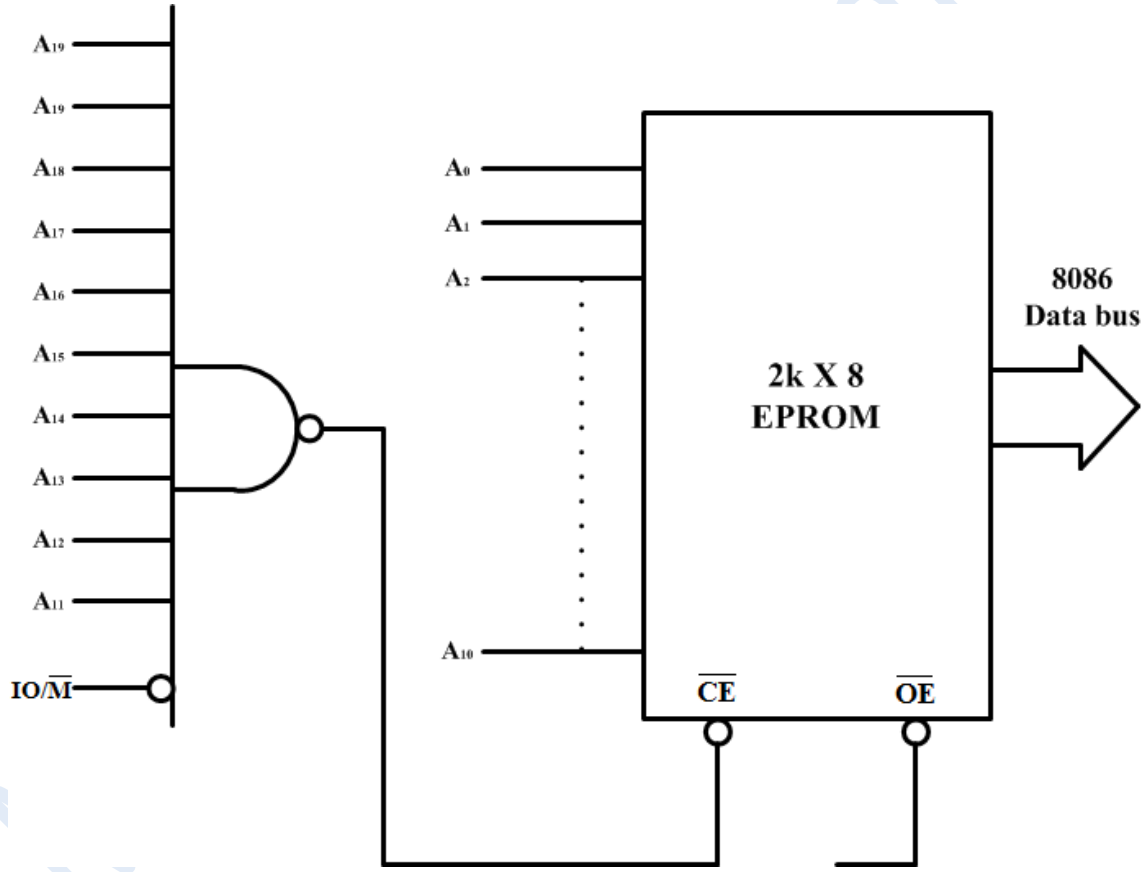

Figure (4.3) ***Single NAND Gate Decoder***

Note that the output of NAND gate is logic 0 whenever all its bits A_{11} to A_{19} are all logic 1 and the $\overline{IO/M}$ is logic 0, this activate the EPROM $\overline{CE}$. Whenever the $\overline{CE}$ is logic 0 data will be read from EPROM if the read signal was activated (logic 0). NAND gates are rarely used to decode memory because each memory device required its own NAND gate decoder.

4.3.2.2 3-to-8 Line Decoder (741S138)

One of the more common integrated circuit decoders found in many microprocessor-based systems is the (741S138) 3-8 line decoder. Figure (4.4) and table (4.1) shows the diagram and the truth table for this decoder.

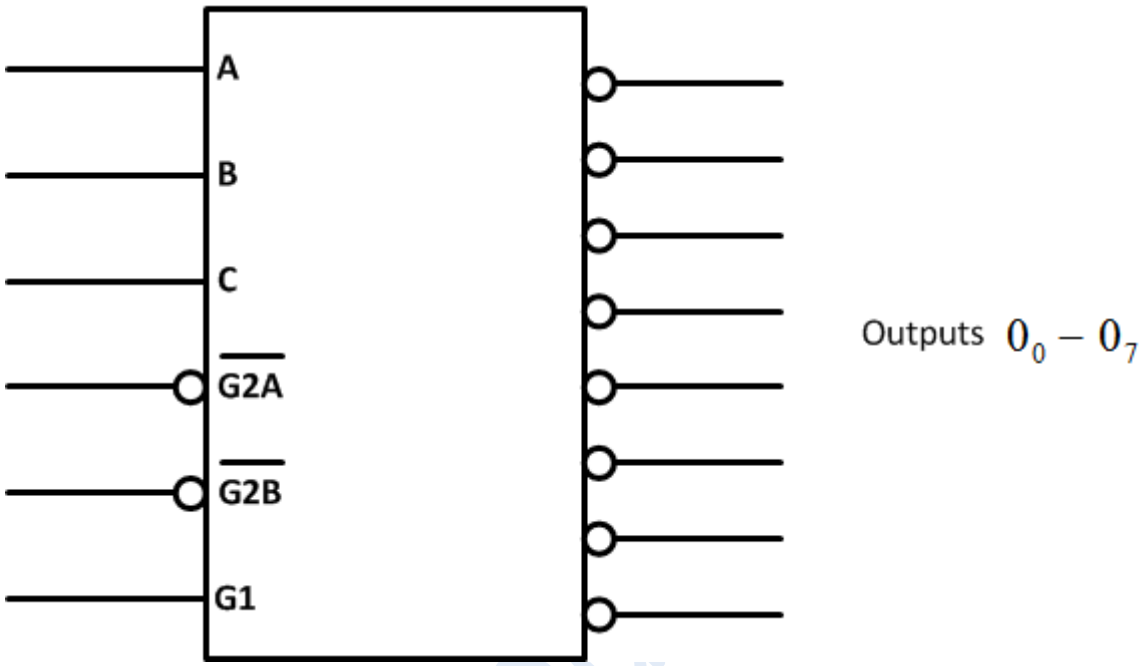

Figure (4.4) ***741S138 decoder***

Input						Outputs							
Enable			Select										
$\overline{G2A}$	$\overline{G2B}$	G1	C	B	A	0	1	2	3	4	5	6	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Table (4.2) ***Truth Table to the 741S138 Decoder***

Note that the output is always only one of the eight outputs ever geos law at any time. For any of the decoder output to go low, the three inputs $\overline{G2A}$, $\overline{G2B}$ and G1 must all be active (0, 0, and 1) respectively. Once the chip is enable the address (C, B, and A) select which output pin goes low.

Example: design a memory map unit to interface a total of 64K byte EPROM memory in the memory address range (F0000h – FFFFFh).

Sol.

No. of EPROM chips required = Total EPROM memory space / Size of the available chip $= \frac{64K \times 8}{8K \times 8} = 8$ chips

Decoder required for the EPROM memory is 2^n=8K ⟶ n=13 ($A_0 – A_{12}$).

Region select = A_{19}, A_{18}, A_{17} and A_{16} .

Chip select = A_{15}, A_{14} and A_{13} .

Location = A_{12}, A_{11}, A_{10}, …….. and A_0.

Since the MP has a 20 bit address lines ($A_0 – A_{19}$) then

1. ($A_0 – A_{12}$) are used to select each location within each EPROM chip.
2. (A_{13}, A_{14}, and A_{15}) are used to select one of the 8 EPROM chips
3. (A_{16}, A_{17}, A_{18} and A_{19}) are used to select the EPROM region.

Figure (4.6) illustrates the memory map interface cct.

The decoder outputs are connected to the $\overline{CE}$ inputs of the EPROMs and the $\overline{RD}$ signal from the 8086 is connected to the $\overline{OE}$ inputs of the EPROMs. This allows only the selected EPROM to be enabled and to send its data to the MP through the data bus whenever $\overline{RD}$ becomes logic 0.

The three inputs NAND gate is connected to address bits $A_{19} – A_{17}$. When all three address inputs are high, the output of the NAND goes low and enables input $\overline{G2B}$ of the 741S138. Input G1 is connected directly to A_{16}. In other words, in order to enable this decoder the last four address connections ($A_{19} – A_{16}$) must be all high.

The address inputs **C**, **B**, and **A** are connected to MP address pins (A_{15} – A_{13}). These three address inputs determine which output goes low and which EPROM is selected.

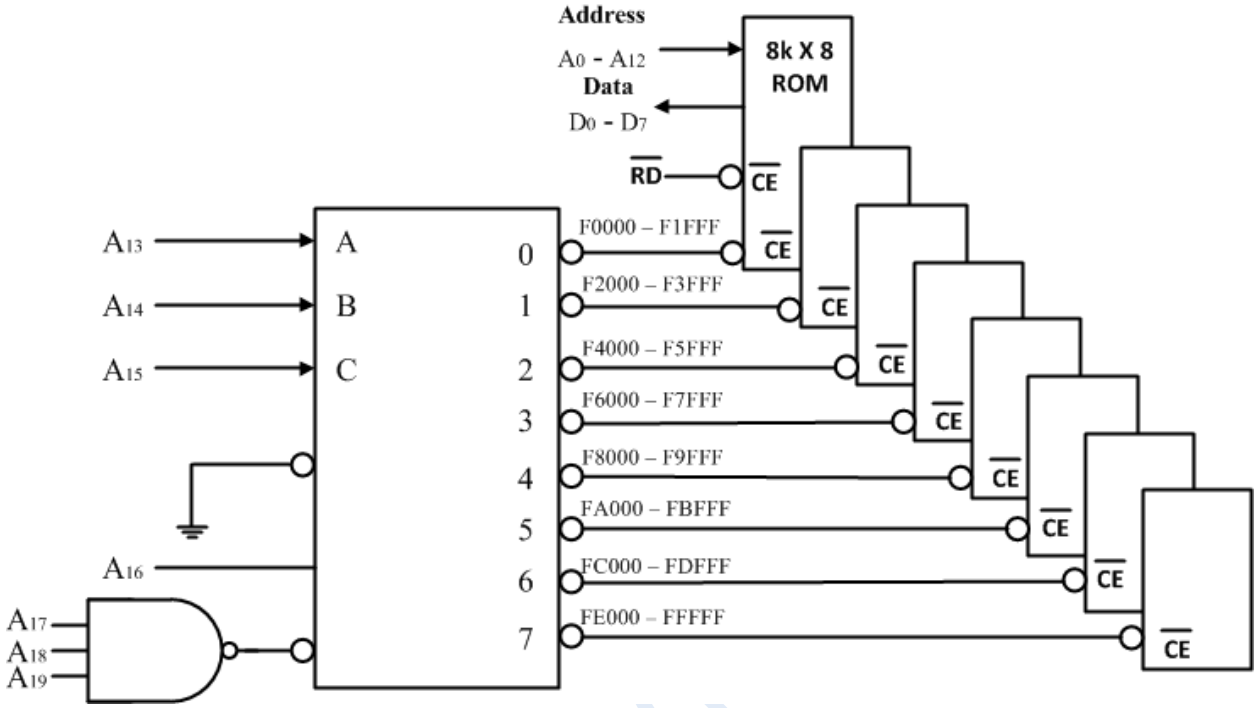

Figure (4.5) ***Memory Map Interface Diagram***