Chapter 2: Logic Gates

A large number of electronic circuits (in computers, control units, and so on) are made up of logic gates. These process signals which represent true or false.

The most common symbols used to represent logic gates are shown below: NOT, AND, OR, NAND, NOR, XOR

2.1 Not Gate (The Inverter)

The inverter (NOT circuit) performs the operation called inversion or complementation. The inverter changes one logic level to the opposite level. In terms of bits, it changes a 1 to a 0 and a 0 to a 1.

Standard logic symbols for the inverter are shown in Fig. (4.1), shows the distinctive shape symbols.

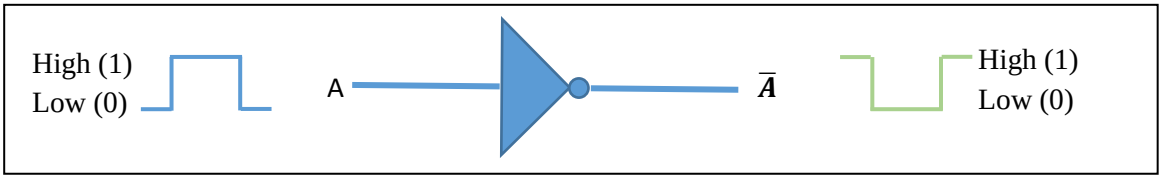

Fig. (2.1) Logic symbol for the inverter.

Y= Input

x = Output

If Y = 0 then x =1

Y = 1 then x = 0

2.2 And Gate

The term gate is used to describe a circuit that performs a basic logic operation. The AND gate is composed of two or more inputs and a single output, as indicated by the standard logic symbols shown in Fig. (4.2). Inputs are on the left, and the output is on the right in each symbol.

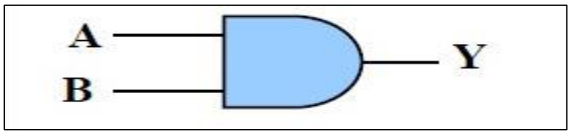

Fig. (2.2) AND gate symbol.

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

The operation can be expressed on equation form as following: If one input is A, the other input is B and the output is X, then the expression for this basic gate function is:

$$X = AB \quad \text{OR} \quad X = A.B$$

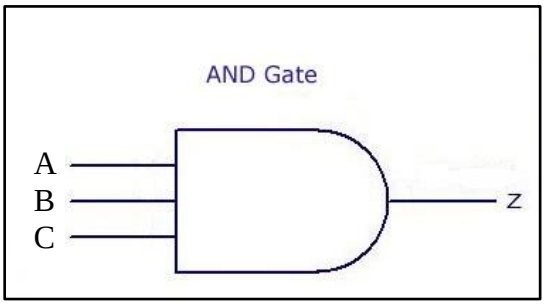

Fig. (2.3) AND gate symbol with three input.

Input			Output
A	B	C	Z= (ABC)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

The Boolean expression for three input W, X and Y and output Z is express by the equation below:

$$Z = ABC \quad \text{OR} \quad Z = A.B.C$$

The total number of possible combinations of binary inputs to a gate is determined by the following formula:

$$N = 2^n$$

Where N is the number of possible input combinations and n is the number of input variables. To illustrate:

For two input variables: $N = 2^2 = 4$ combinations.

For three input variables: $N = 2^3 = 8$ combinations.

For four input variables: $N = 2^4 = 16$ combinations.

Operation with Waveform Inputs

Let's examine the waveform operation of an AND gate by looking at the inputs with respect to each other in order to determine the output level at any given time. In Fig. (4.4), inputs A and B are both HIGH (1) during the time interval, t1 making output X HIGH (1) during this interval. During time interval t2 input A is LOW (0) and input B is HIGH (1), so the output is LOW (0). During time interval t3, input A is HIGH (1) and input B is LOW (0), resulting in a LOW (0) output. Finally, during time interval t4, both inputs are LOW (0), and therefore the output is LOW (0). As you know, a diagram of input and output waveforms showing time relationships is called a timing diagram.

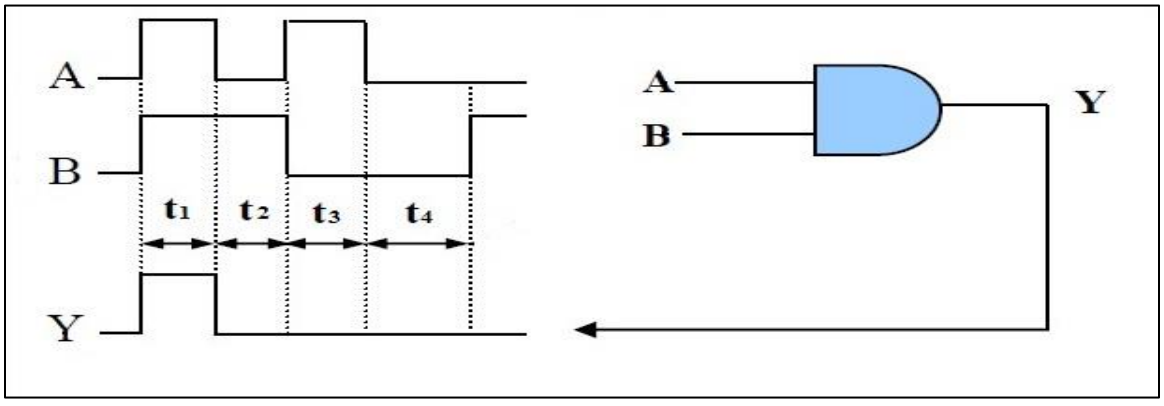

Fig. (2.4) Example of AND gate operation with a timing diagram showing input and output relationships.

2.3 OR Gate

An OR gate can have more than two inputs. The OR gate is another of the basic gates from which all logic functions are constructed. An OR gate can have two or more inputs and performs what is known as logical addition. An OR gate has two or more inputs and one output, as indicated by the standard logic symbol in Fig. (4.5), where OR gates with two inputs are illustrated. An OR gate can have any number of inputs greater than one.

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

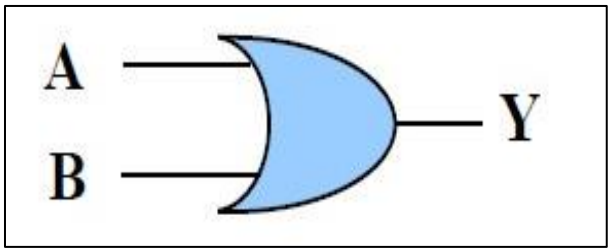

Fig. (2.5) Standard logic symbol for the OR gate.

The operation of a 2-input OR gate can be expressed as follows: If one input variable is A, if the other input variable is B, and if the output variable is X, then the Boolean expression is:

$$X = A + B$$

The Boolean expression for three input A, B and C and output X is express by the equation below:

$$X = A + B + C$$

Operation with Waveform Inputs

Now let's look at the operation of an OR gate with pulse waveform inputs, keeping in mind its logical operation. Again, the important thing in the analysis of gate operation with pulse waveforms is the time relationship of all the waveforms involved. For example, in Fig. (4.6), inputs A and B are both HIGH (1) during time interval t1 making output X HIGH (1). During time interval t2, input A is LOW (0), but because input B is HIGH (1), the output is HIGH (1). Both inputs are LOW (0) during time interval t3, so there is a LOW (0) output during this time. During time interval t4, the output is HIGH (1) because input A is HIGH (1).

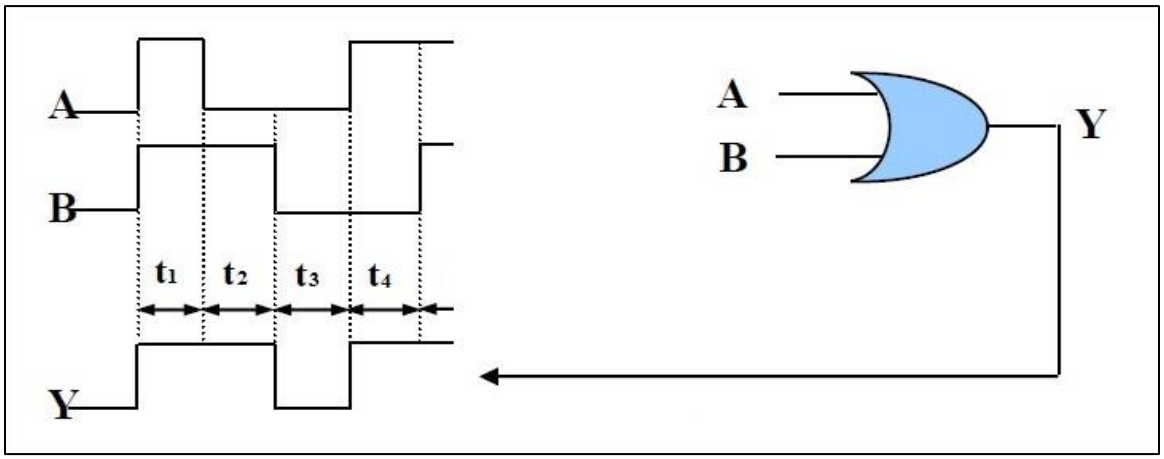

Fig. (2.6): Example of OR gate operation with a timing diagram showing input and output relationships.

2.4 The NAND Gate

The NAND gate is a popular logic element because it can be used as a universal gate: that is, NAND gates can be used in combination to perform the AND, OR, and inverter operations.

The term NAND is a contraction of NOT-AND and implies an AND function with a complemented (inverted) output. The standard logic symbol for a 2-input NAND gate and its equivalency to an AND gate followed by an inverter are shown in Fig. (4.7) (a), where the symbol ≡ means equivalent to. A rectangular outline symbol is shown in part (b).

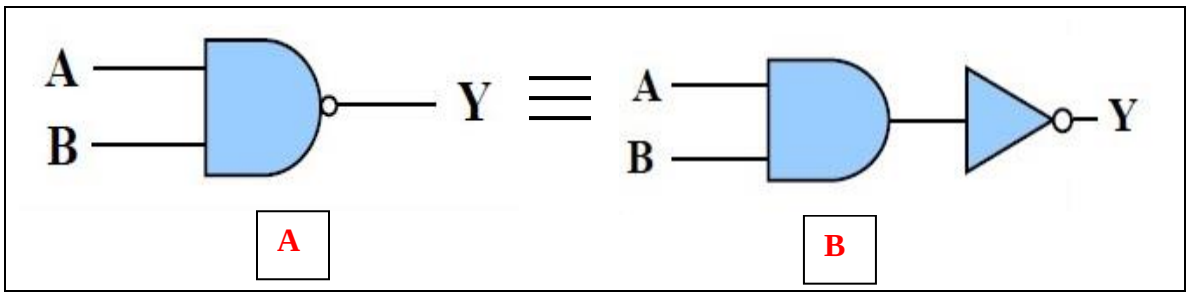

Fig. (2.7) Standard logic symbol for the NAND gate.

Logic Expressions for a NAND Gate

The Boolean expression for the output of a 2-input NAND gate is

$$X = \overline{AB}$$

This expression says that the two input variables, A and B, are first AND then complemented, as indicated by the bar over the AND expression. This is a description in equation form of the operation of a NAND gate with two inputs. Evaluating this expression for all possible values of the two input variables, you get the results shown in Table below:

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

2.5 The NOR Gate

The NOR gate, like the NAND gate, is a useful logic element because it can also be used as a universal gate; that is, NOR gates can be used in combination to perform the AND, OR, and inverter operations. The term NOR is a contraction of NOT-OR and implies an OR function with an inverted (complemented) output. The standard logic symbol for a 2-input NOR gate and its equivalent OR gate followed by an inverter are shown in Fig. (4.8).

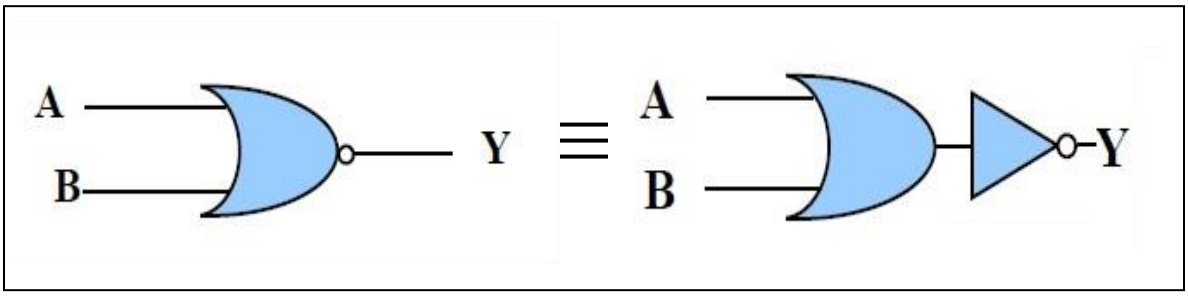

Fig. (2.8) Standard NOR gate logic symbols.

Logic Expressions for a NOR Gate

The Boolean expression for the output of a 2-input NOR gate can be written as

$$X = \overline{A + B}$$

This equation says that the two input variables are first OR and then complemented, as indicated by the bar over the OR expression. Evaluating this expression, you get the results shown in Table below. The NOR expression can be extended to more than two input variables by including additional letters to represent the other variables.

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

2.6 Exclusive -OR gate

Standard symbol for an exclusive-OR (XOR for short) gate is shown in Fig. (4.9). The XOR gate has only two inputs.

Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

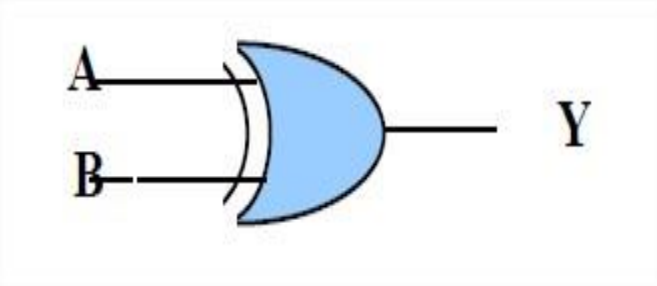

Fig. (2.9) Standard symbol for an exclusive-OR.

Logic Expressions for a XOR Gate

The Boolean expression for the output of a 2-input NOR gate can be written as

$$Y = \bar{A}B + A\bar{B}$$

$$Y = A \oplus B$$

2.7 Exclusive -NOR gate

Standard symbols for an exclusive-NOR (XNOR) gate are shown in Fig. (4.10). Like the XOR gate, an XNOR has only two inputs. The bubble on the output of the XNOR symbol indicates that its output is opposite that of the XOR gate. When the two input logic levels are opposite, the output of the exclusive-NOR is gate LOW. The operation can be stated as follows (A and B are inputs, X is the output):

Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

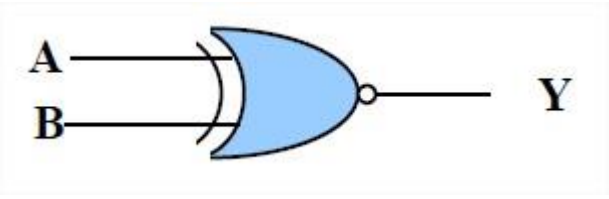

Fig. (4.10) Standard symbol for an exclusive-NOR.

Logic Expressions for a XNOR Gate

The Boolean expression for the output of a 2-input NOR gate can be written as

$Y = AB + \bar{A}\bar{B}$

$Y = A \odot B$

Example:

Determine the output waveforms for the XOR gate and for the XNOR gate, given the input waveforms, A and B, in Figure below: