Chapter 6: Counters and Registers

6.1 Counters

One common requirement in digital circuits is counting, both forward and backward. Digital clocks and watches are everywhere, timers are found in a range of appliances microwave ovens and counters for other reasons are found in everything from automobiles to test equipment. Counters are composed of flip-flops, which are used for measurement of frequency and time period, sequencing of equipment operation, frequency division and mathematical manipulation in digital equipment. A counter is a sequential circuit that counts. In digital logic and computing, a counter is a device which stores the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are classified into two broad categories according to the way they are clocked. They are: (i) Asynchronous or Ripple counter. and (ii) Synchronous counter.

One flip flop used to count w possible state (0 & 1), two flip flop used to count 4 possible state (00 to 11).

So $N=n^2$

Where: N= Maximum number of counter state, n= Number of flip flop used in counter

3 f.f = 2^3 = 8 states (000 to 111)

4 f.f = 2^4 = 16 states (0000 to 1111)

1. Asynchronous counter (ripple counter)

The first flip flop is clocked by external clock pulse, and then each successive flip flop is clocked by the output of preceding flip flop.

2. Synchronous counter

Synchronous counter have a common clock for all flip flop. The clock input is connected to all flip flop so that they are clocked at the same time (simultaneously).

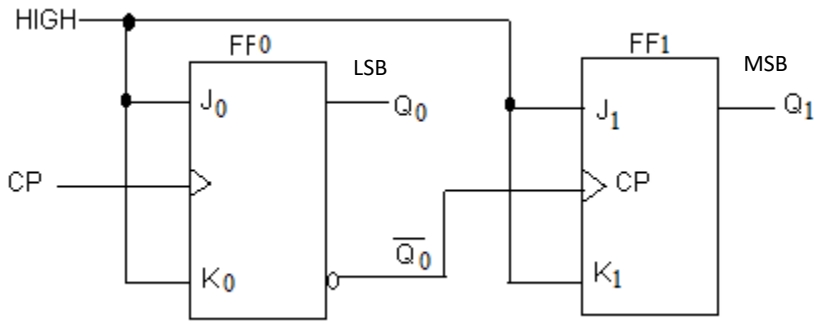
Asynchronous counter (ripple counter)

Ex: Design 2 bit an asynchronous binary counter using J-k f.f using positive edge.

Solution:

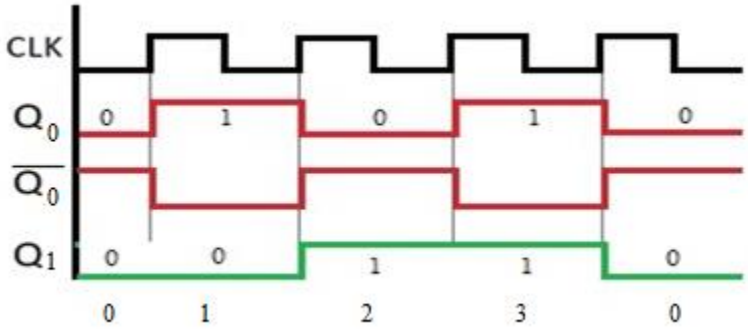
2 bit need 2 f.f , No. of count sequence $=2^n$

n= no. of f.f , $N= 2^2 = 4$ states



Binary state sequence for 2 bit counter:

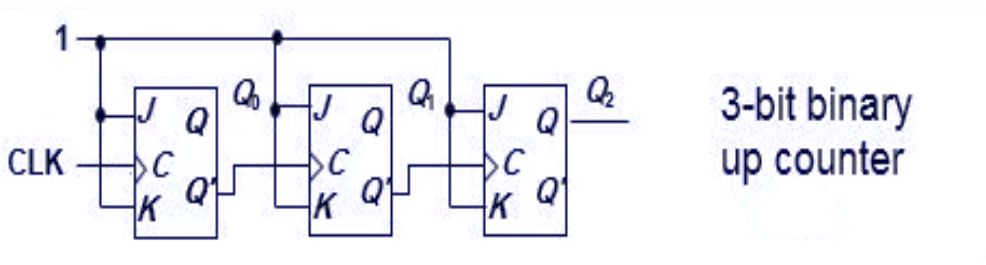
Q_1	Q_0
0	0
0	1
1	0
1	1



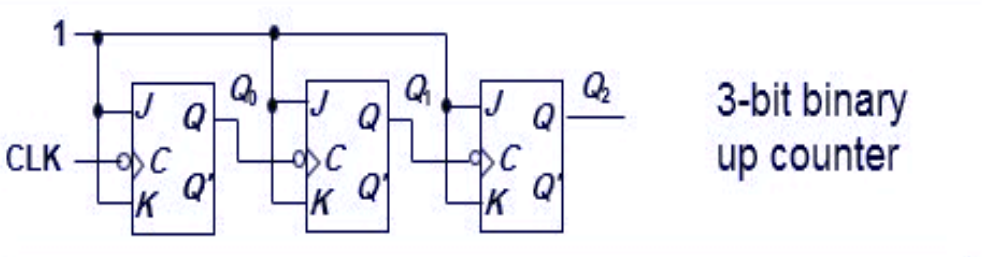
This counter is called mod 4 mean count from 0 to 3 (00 to 11).

Note:

1. If we use positive clock and the counter count up we connect the first f.f $\overline{Q}$ to the next f.f clock and so on. If we use negative clock and the counter count up we connect the first f.f Q to the next f.f clock and so on.

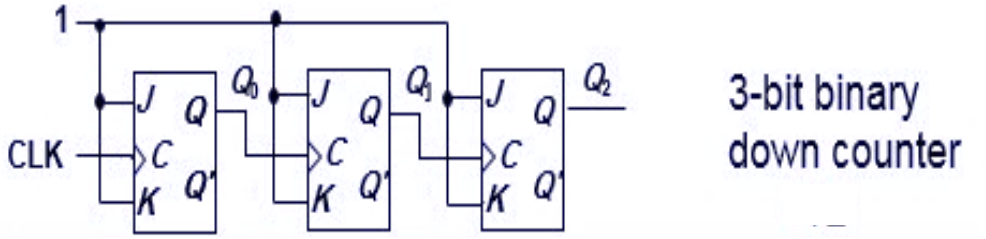


3-bit binary up counter

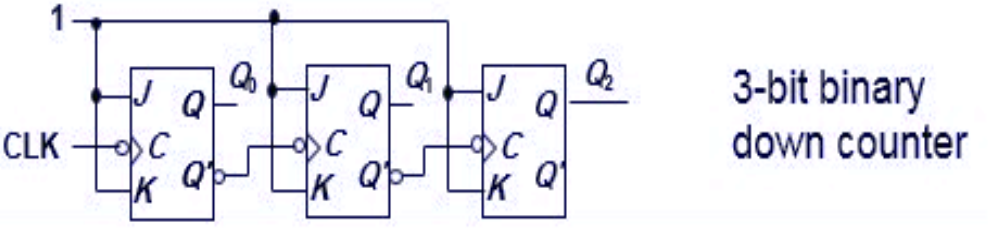


3-bit binary up counter

2. If we use positive clock and the counter count down we connect the first f.f Q to the next f.f clock and so on. If we use negative clock and the counter count down we connect the first f.f $\overline{Q}$ to the next f.f clock and so on.



3-bit binary down counter



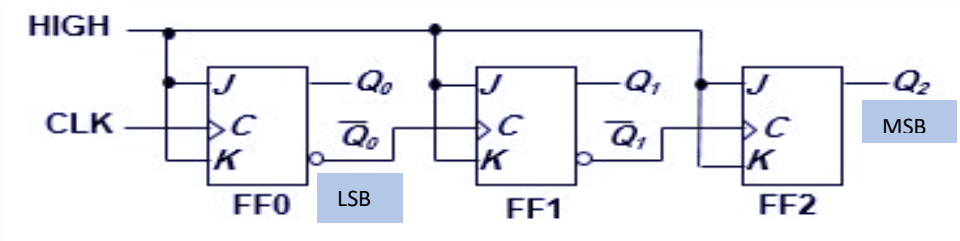
3-bit binary down counter

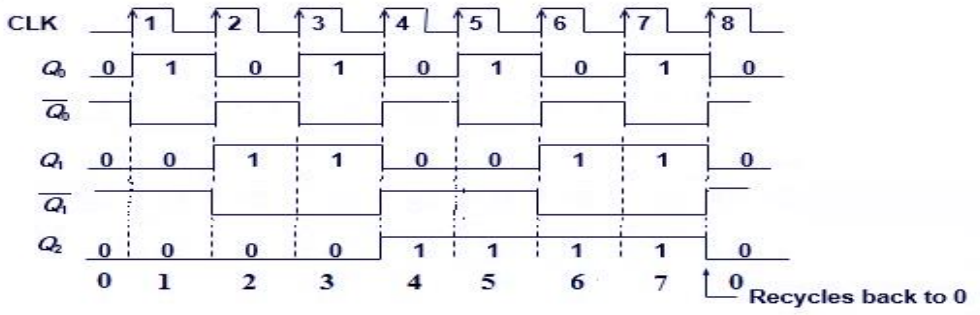
Ex: Design 3 bit an asynchronous binary ripple counter using J-k f.f operate by positive edge.

Solution:

3 bit need 3 f.f , No. of count sequence $=2^n$

n= no. of f.f , $N= 2^3 = 8$ states

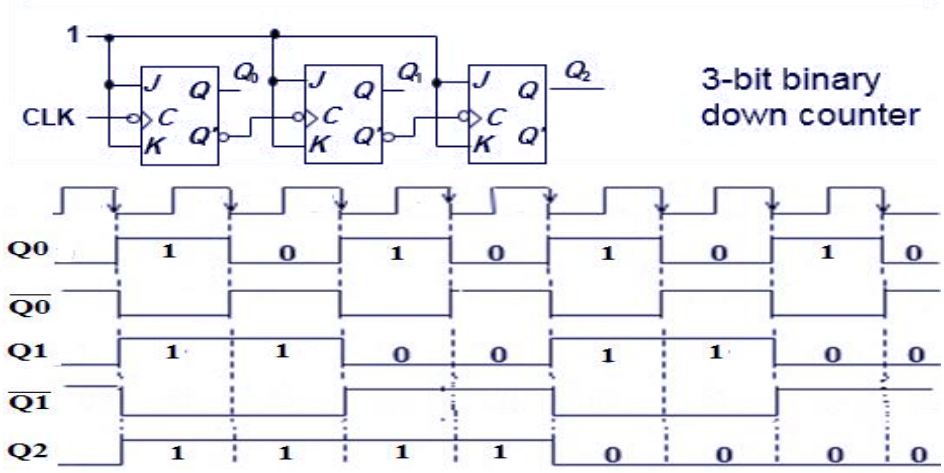




Ex: Design 3 bit an asynchronous binary down counter using J-k f.f operate by negative edge. Solution:

3 bit need 3 f.f , No. of count sequence $=2^n$

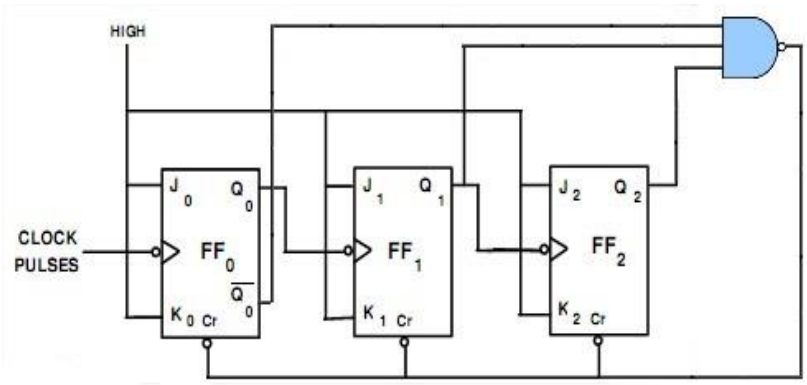
n= no. of f.f , $N= 2^3 = 8$ states



Ex: Design an asynchronous counter that count from 0 to 5 (mod-6) using J-k f.f operate by (-ve) edge.

Solution:

- Count sequence from 0 to 5, so need 3 f.f.
- This means the counter after reach No.5 must return to zero.
- (-ve) edge means, the first f.f take the (-ve) clock, the second f.f take the clock from Q_0 and the third f.f take the clock from Q_1,
- Mod-6 counter means (6 = 1 1 0) so connect $\overline{Q0}$, $Q1$ and $Q2$ to NAND gate input and the output goes to the clear input in each f.f.



Homework: Design an asynchronous counter that count from 0 to 6 (mod-7) using J-k f.f.

Synchronous counter

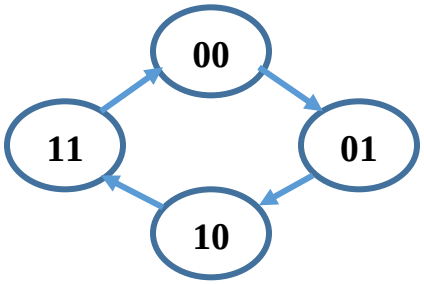
To design a synchronous counter follow this rules:-

1- State diagram.
2- Next state table.
3- Flip flop excitation table.
4- K.map
5- Logic expression
6- Counter implementation.

Ex: Design a synchronous counter which can count number (0, 1, 2, 3) using J-k f.f operate by (-ve) edge.

Solution:

1- State diagram.



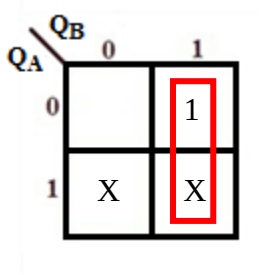
2- Next state table.

3- Flip flop excitation table.

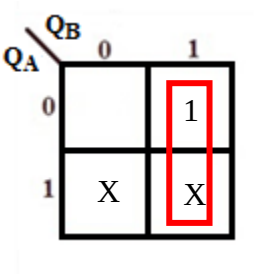
Present State		Next State		Flip Flop Input			
Q_A	Q_B	Q_A	Q_B	J_A	K_A	J_B	K_B
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

4- K.map

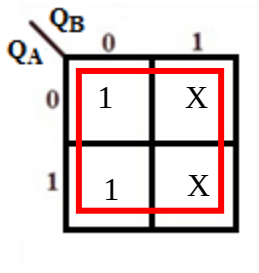
5- Logic expression



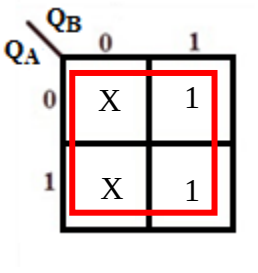
$J_A=Q_B$



$K_A=Q_B$

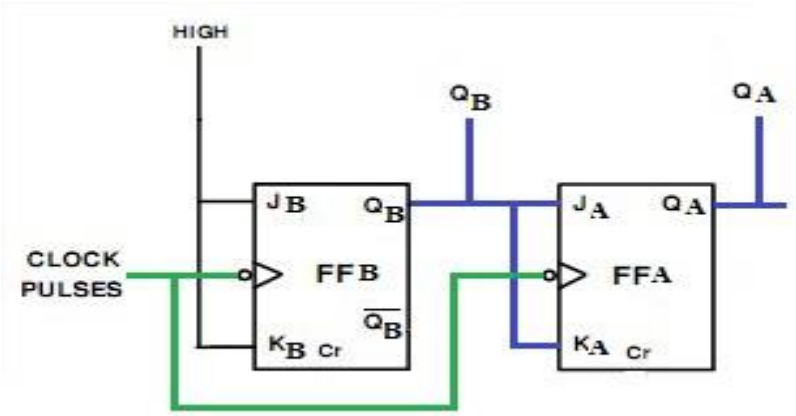


$J_B=1$



$K_B=1$

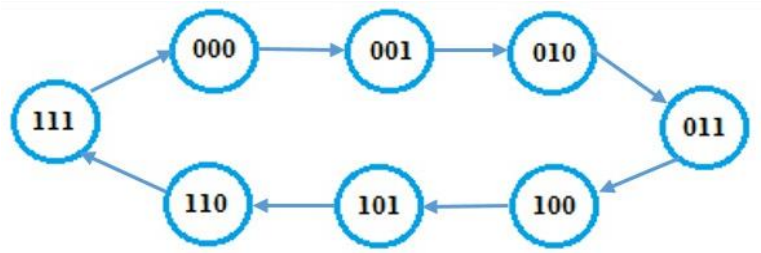
6- Counter implementation.



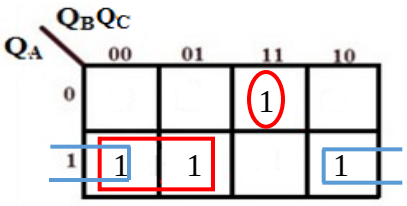
Ex: Design mod-8 binary synchronous counter using D- f.f operate by (-ve) edge.

Solution:

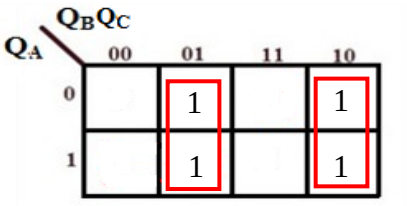
0 ⟶ 7 mod – 8 $8=2^3$ ⟹ n=3 No of f.f



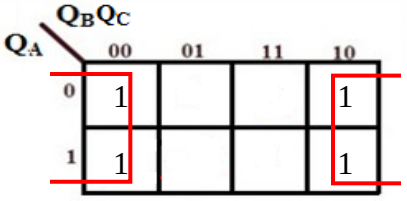
Present State			Next State			Flip Flop Input		
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C	D_A	D_B	D_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0



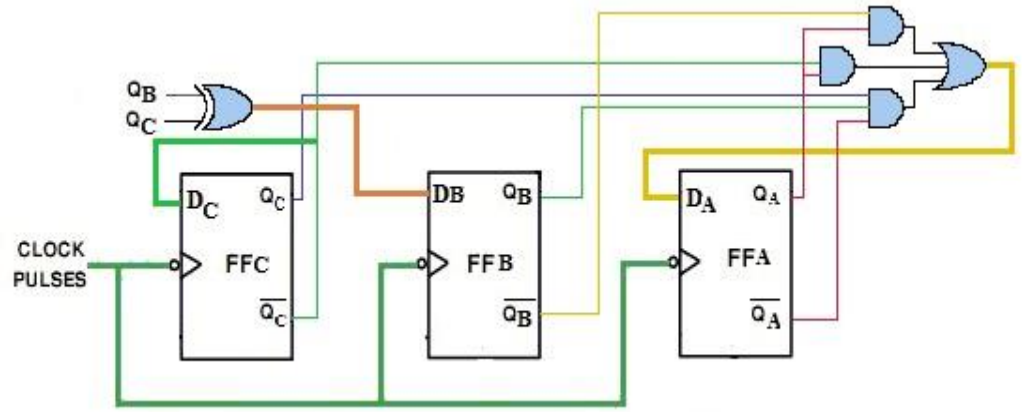
$D_A= \overline{QA}Q_BQ_C + Q_A\,\overline{QB} + Q_A\,\overline{QC}$



$D_B=\overline{QB}Q_C + Q_B\,\overline{QC} = Q_B \oplus Q_C$

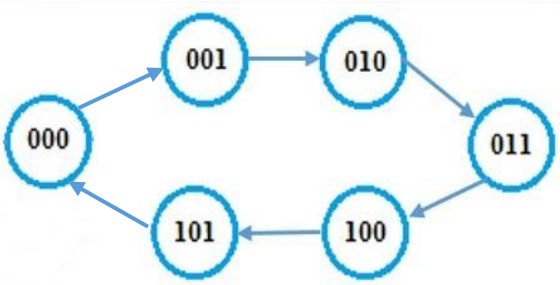


$D_C=\overline{QC}$

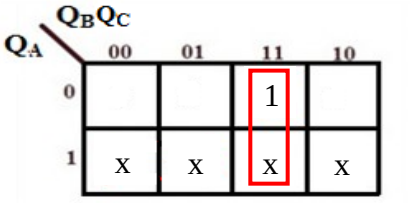


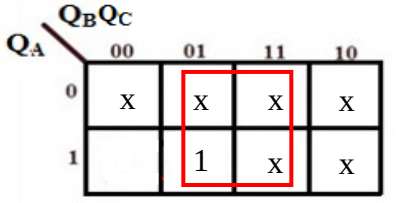
Ex: Design synchronous counter that can count number (0, 1, 2, 3, 4, 5) using J-K f.f operate by (-ve) edge.

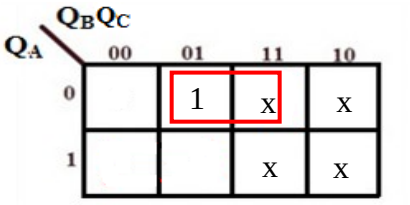
Solution:

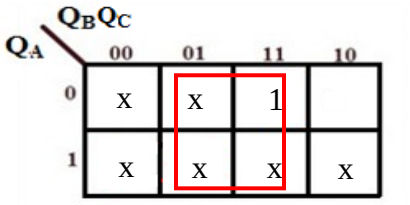


Present State			Next State			Flip Flop Input					
Q_A	Q_B	Q_C	Q_A	Q_B	Q_C	J_A	k_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x



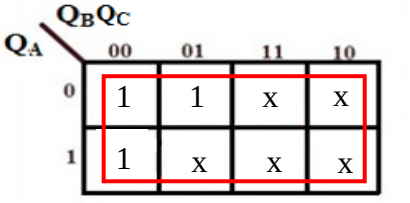


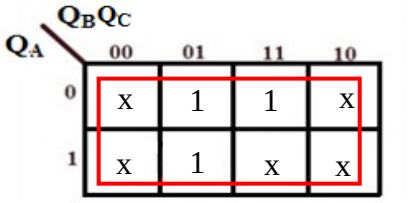




$J_B=\overline{QA}Q_C$

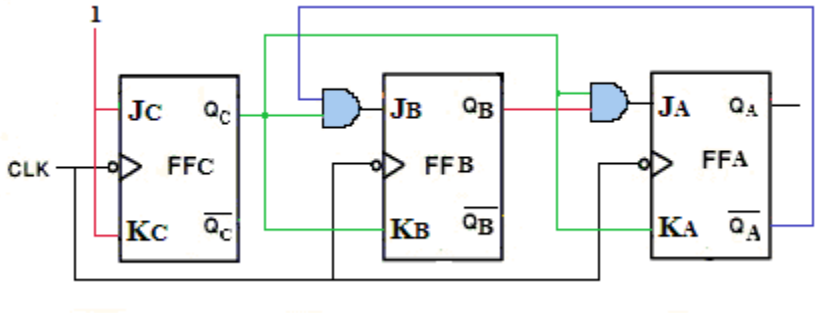
$K_B=Q_C$





$J_C=1$

$K_C=1$



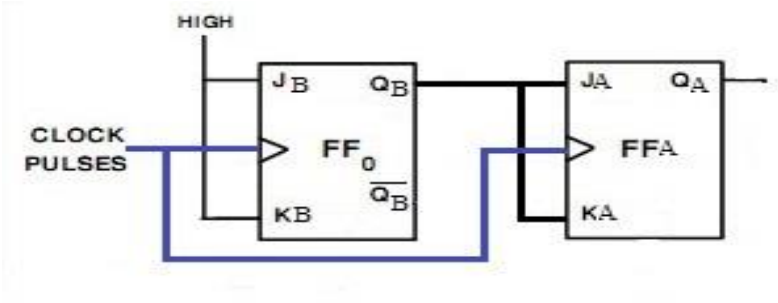
Homework:

1- Design synchronous counter that can count No. (0, 1, 2, 5, 10, 3, 13, 15) using T f.f operate by (-ve) edge.

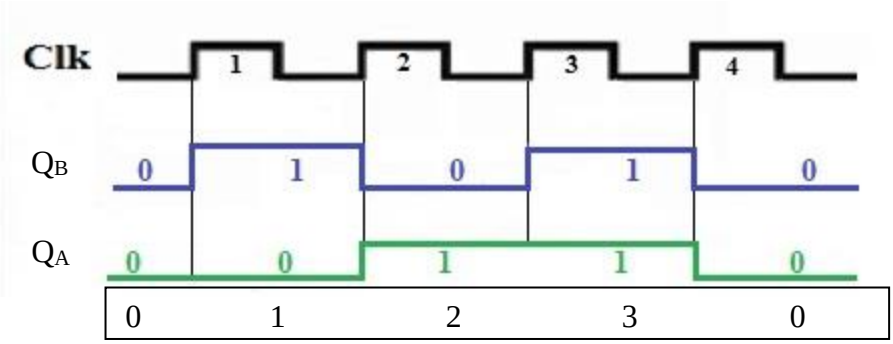
2- Design a BCD decade synchronous counter using R-S f.f operate by (-ve) edge.

Synchronous counter operation

Ex: For the synchronous counter in figure below, draw the timing diagram for 4 clock & find which number this counter can count?

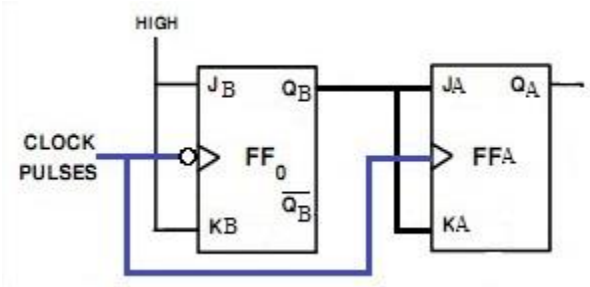


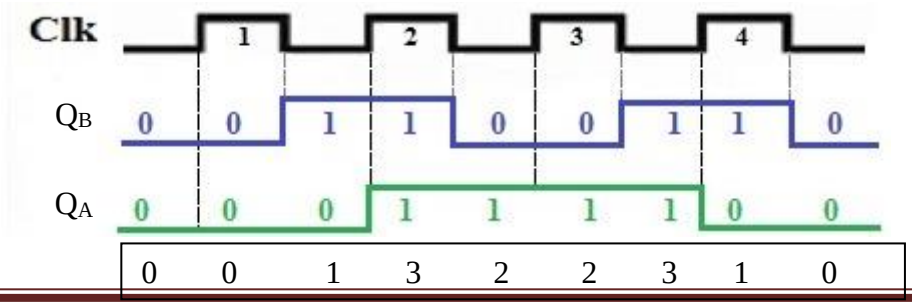
Solution:



Ex: For the synchronous counter in figure below, draw the timing diagram for 4 clock & find which number this counter can count?

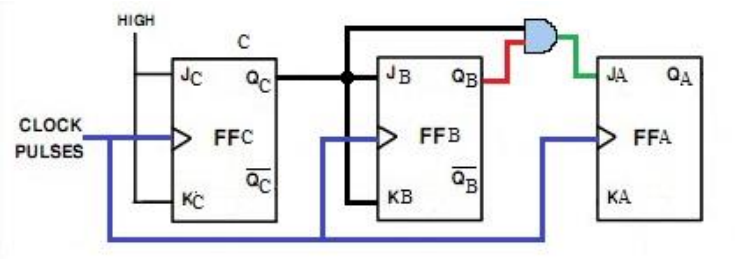
Solution:

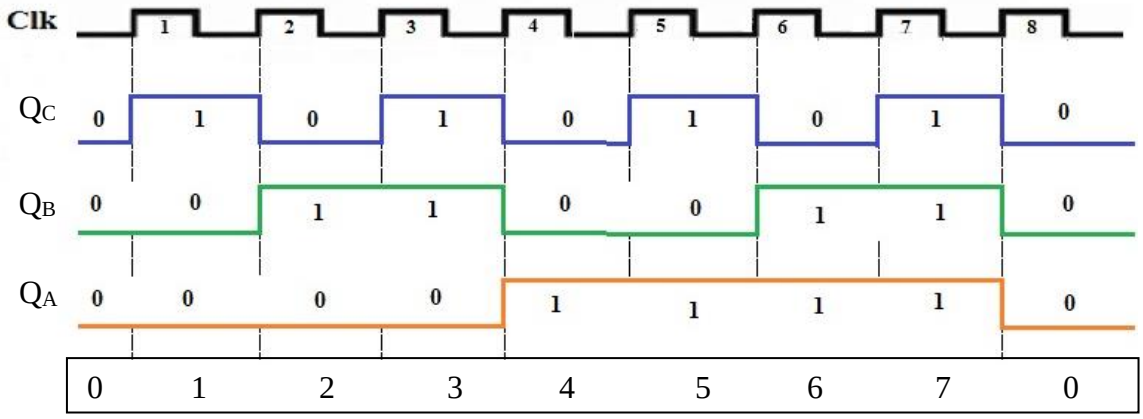




Ex: For the synchronous counter in figure below, draw the timing diagram for 8 clock & find which number this counter can count?

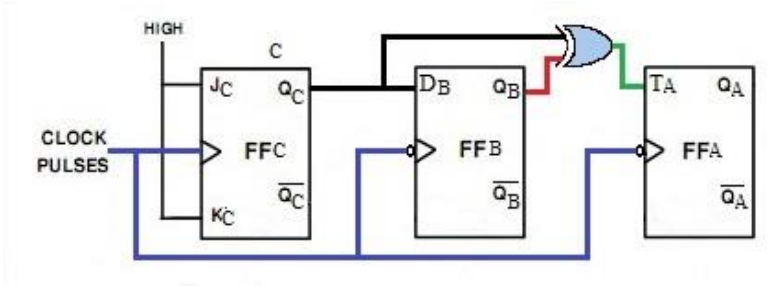
Solution:

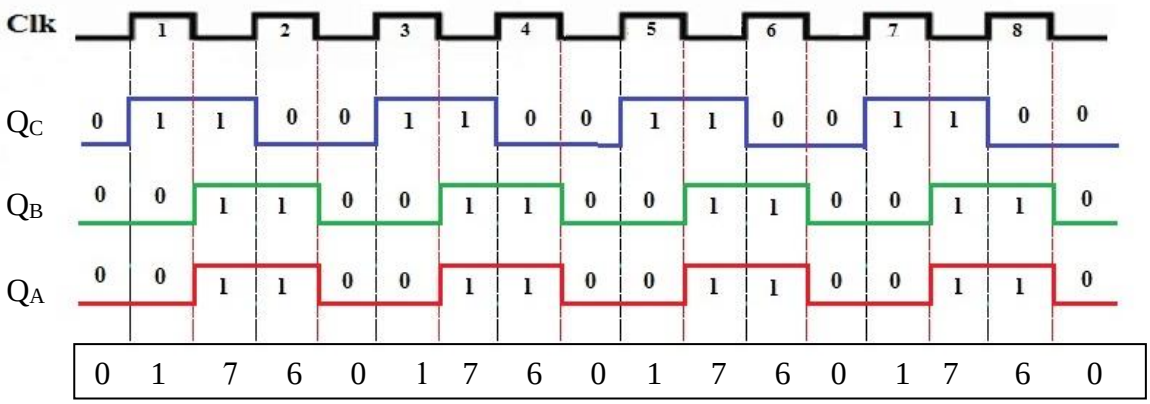




Ex: For the synchronous counter in figure below, draw the timing diagram for 8 clock & find which number this counter can count?

Solution:





6.2 Shift register

The other important application of f.f is shift register. The shift register is a digital circuit with two basic function:

a) Data storage

b) Data movement

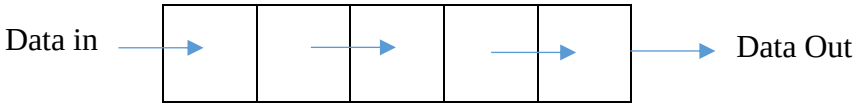
The storage capability of a register makes it an important type of memory device. The shift register (data movement) consists of an arrangement of flip flop and are important in application involving the storage and transfer of data in digital system.

Registers are implement with flip flop, the shift capability of a register permits the movement of data form stage to stage within the register or into or out of the register upon application of clock pulses.

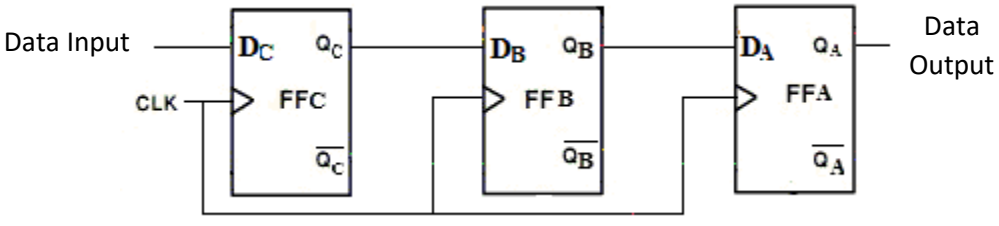
There are many types of shift register:

1) Serial in Serial out (SISO).
2) Serial in Parallel out (SIPO).
3) Parallel in Serial out (PISO).
4) Parallel in Parallel out (PIPO).
5) Rotate shift register.

1) Serial in Serial out (SISO)

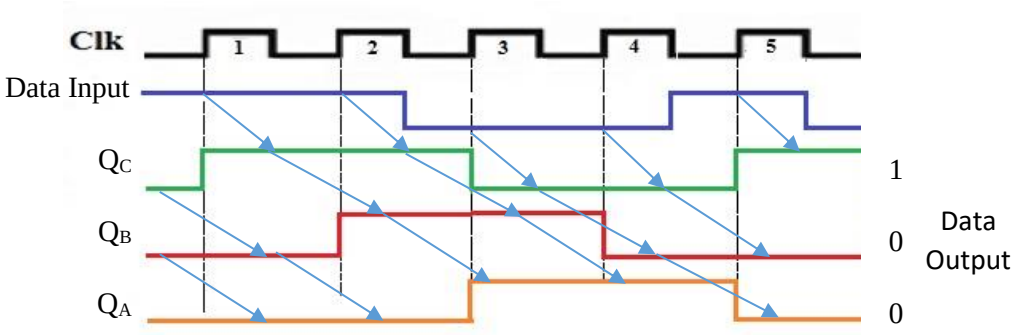


This type of register accepts data serially that is one bit at a time on a single time. It produces the stored information on its output also in serial form.



Example: Show the state of shift register for the input waveform (ClK & Data input) given below for 5 clock. Assume that the register is initially all 0's.

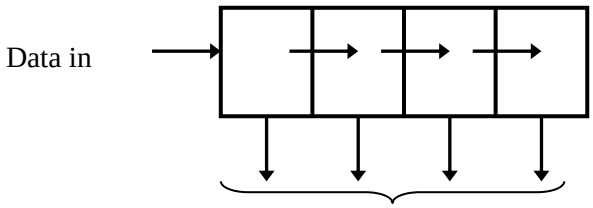
Solution:

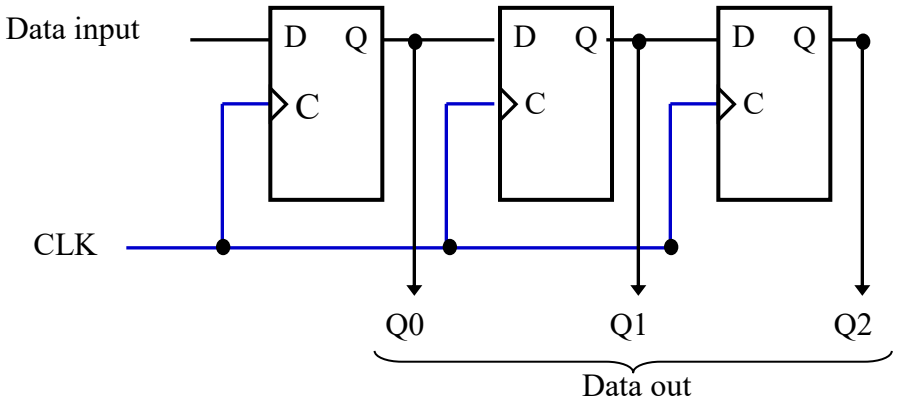


Homework: For the input waveform given above what is the output of the shift register (3 bit) after five clock pulses if the initially state (011).

2) Serial in Parallel out (SIPO).

In this type of register data bits are serially leaded but the output of the register is taken in parallel as shown bellows.

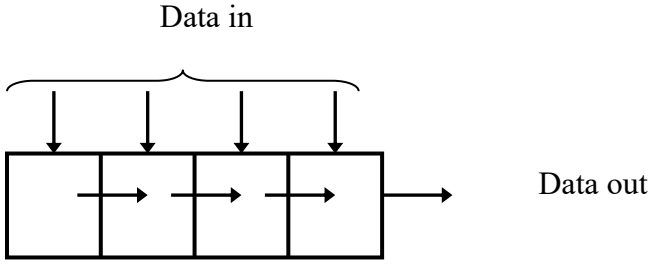


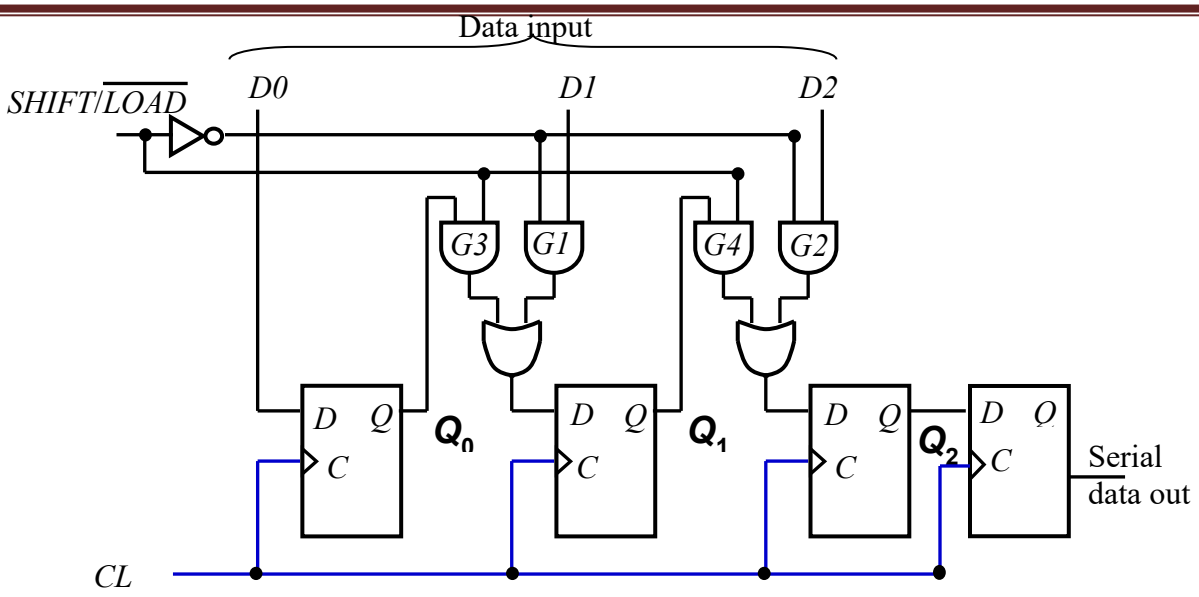


3-bits serial in –parallel out register

3) Parallel in Serial out (PISO).

In this type of register the input data are entered simultaneously at the same time but the output of the register is taken in serial as shown bellows.



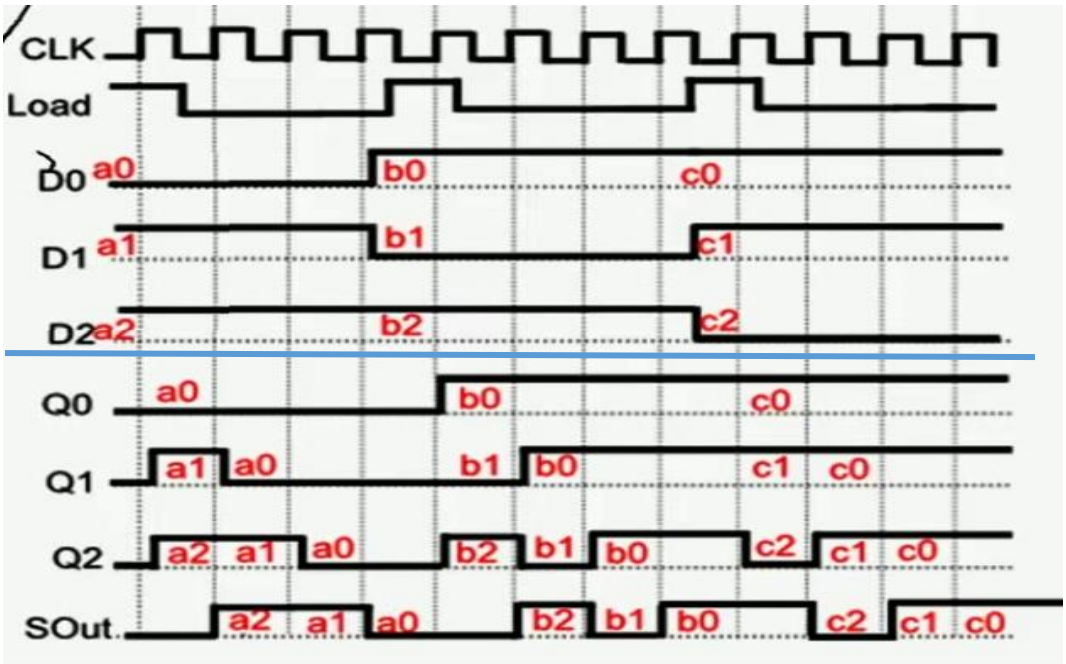


$SHIFT/\overline{LOAD} = S/\bar{L} = 0$, mean *storing data* in parallel $D_0D_1D_2$, and G1 & G2 are active.

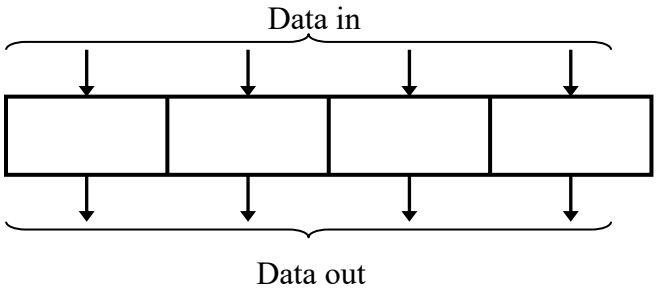
$SHIFT/\overline{LOAD} = S/\bar{L} = 1$, mean *shift* the data on the register and G3 & G4 are active.

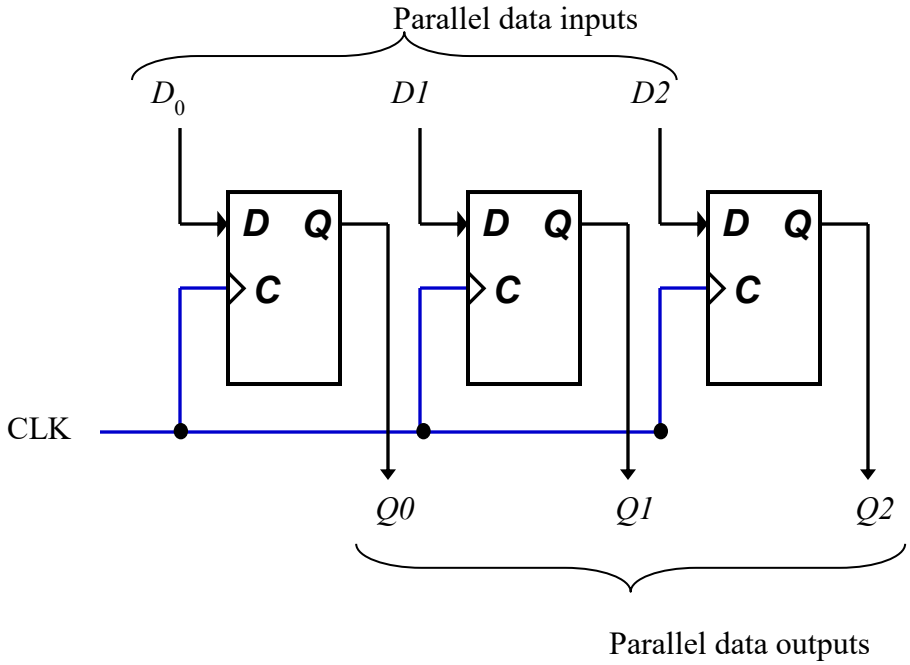
EX: Draw the level waveform for the flip flop output Q0, Q1 and Q2 if the input are given in fig below.

Solution:

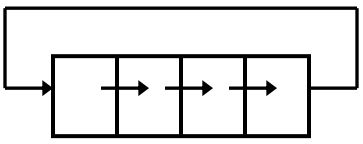


4) Parallel in Parallel out (PIPO).

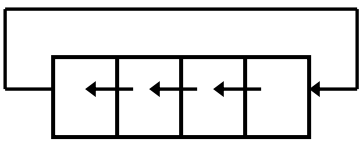




5) Rotate shift register.



Rotate right

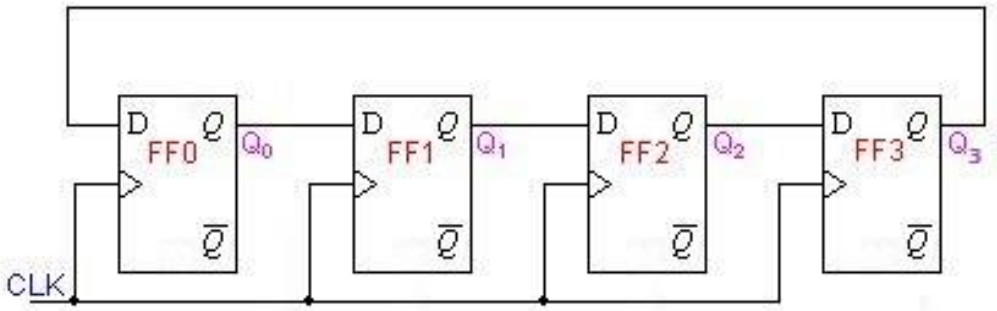


Rotate left

Two of the most common types of shift register counters are introduced here: the *Ring counter* and the *Johnson counter*. They are basically shift registers with the serial outputs connected back to the serial inputs in order to produce particular sequences. These registers are classified as counters because they exhibit a specified sequence of states.

Ring Counters

A ring counter is basically a circulating shift register in which the output of the most significant bit is fed back to the input of the least significant bit. The following is a 4-bit ring counter constructed from D flip-flops. The output of each stage is shifted into the next stage on the positive edge of a clock pulse.

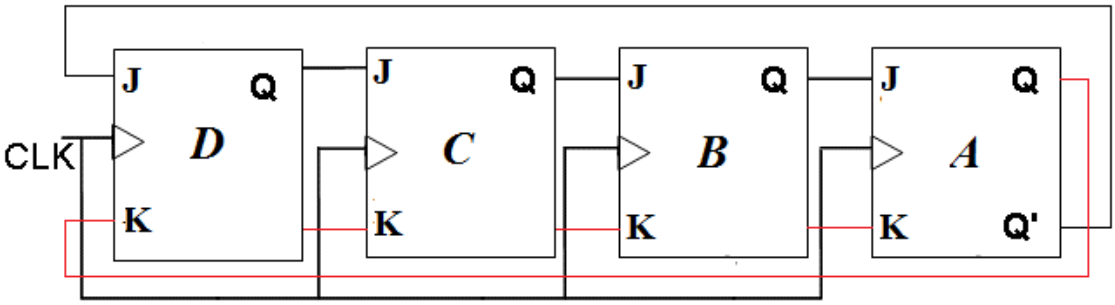


Clock Pulse	Q0	Q1	Q2	Q3
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

Since the count sequence has 4 distinct states, the counter can be considered as a mod-4 counter. Only 4 of the maximum 16 states are used, making ring counters very inefficient in terms of state usage. But the major advantage of a ring counter over a binary counter is that it is self-decoding. No extra decoding circuit is needed to determine what state the counter is in.

Johnson counter

Johnson counters are a variation of standard ring counters, with the inverted output of the last stage fed back to the input of the first stage. They are also known as twisted ring counters. An *n*-stage Johnson counter yields a count sequence of length *2n*, so it may be considered to be a mod-*2n* counter. The circuit above shows a 4-bit Johnson counter. The state sequence for the counter is given in the table as well as the animation on the left.



Clock Pulse	Q0	Q1	Q2	Q3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Again, the apparent disadvantage of this counter is that the maximum available states are not fully utilized. Only eight of the sixteen states are being used.

Note: That for both the Ring and the Johnson counter must initially be forced into a valid state in the count sequence because they operate on a subset of the available number of states. Otherwise, the ideal sequence will not be followed.